Effects Of Temperature On Thyristor Performance

Application Note

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The junction temperature (T_j) of a power semiconductor in any particular situation profoundly affects its performance and reliability. During its working life a thyristor can experience a wide range of temperatures.

Operating at –40˚C is not damaging but allowance must be made by the user for increased gate trigger current, latching current and holding current as well as slow turn-on (see application note AN4840 Gate Triggering and Gate Characteristics). Working in the range between room temperature and 125˚C gives the best compromise between ease of operation and operational life.

T_j = 125˚C is chosen as the design maximum value since above this, blocking current starts to increase rapidly, thus degrading voltage rating, see fig.1.

The device becomes much more susceptible to over-voltage transients , high dv/dt, di/dt and surge current. In the case of the forward blocking junction there is an increasing chance of forward breakover triggering. For special applications it is possible to select devices to operate continuously with low leakage at T_j = 140˚C but such devices may need to be fully characterised and rated on other parameters at 140˚C.

Many applications involve infrequent current overloads for short periods and it is possible to allow T_j to rise well above 125˚C in such situations. A typical situation is during a load short circuit when the device is protected by a fuse. In 50Hz circuits the thyristor may often have to carry short circuit current for up to 10ms. During this time T_j can rise transiently to 300 - 500˚C without the junction being damaged. Peak temperature lags peak current by typically 2 or 3 milliseconds and, although falling, is still high at the end of the current pulse. If current is interrupted by a fuse, little or no reverse voltage appears across the device. However, the re-application of reverse voltage at such a high temperature can result in very high reverse recovery power dissipation. This escalates the junction temperture further and the subsequent high blocking current leads to reverse voltage failure by thermal runaway.

Limit case surge currents are determined by experimental means using a 50Hz half sine of current and published in the data sheet. These I_{TSM} limit values are used to determine the peak temperature (Using I_{TSM} for V_R=0) and the temperature at the end of the current loop (Using I_{TSM} for V_R = 50% V_{RRM}). These temperatures are then taken as the limit temperatures for the particular device. If temperatures in other applications are kept below these, then the condition will be safe.

The method of calculating overload T_j for the published I_{TSM} currents and other overload conditions is discussed below.

The overload above assumed a high speed fuse or circuit breaker will interrupt the supply before forward blocking voltage appears. Some overloads require that the device survives with

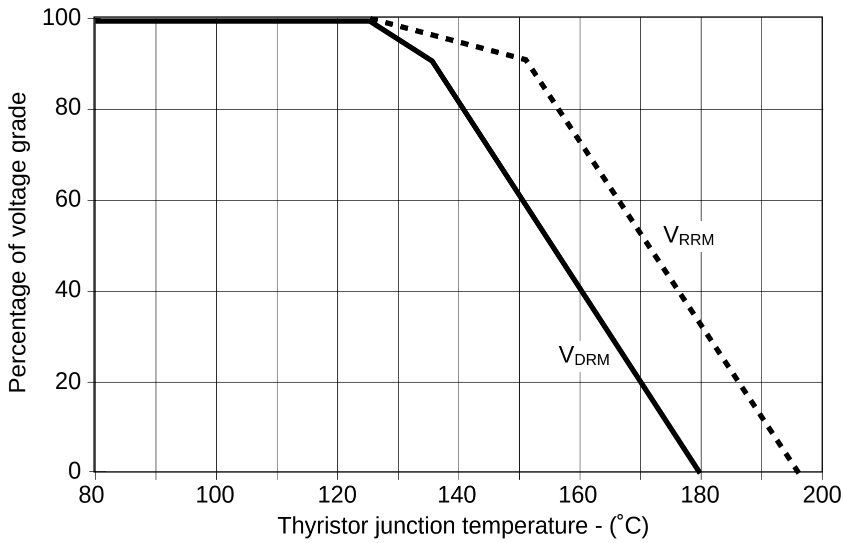

Fig.1 Thyristor de-rating curves

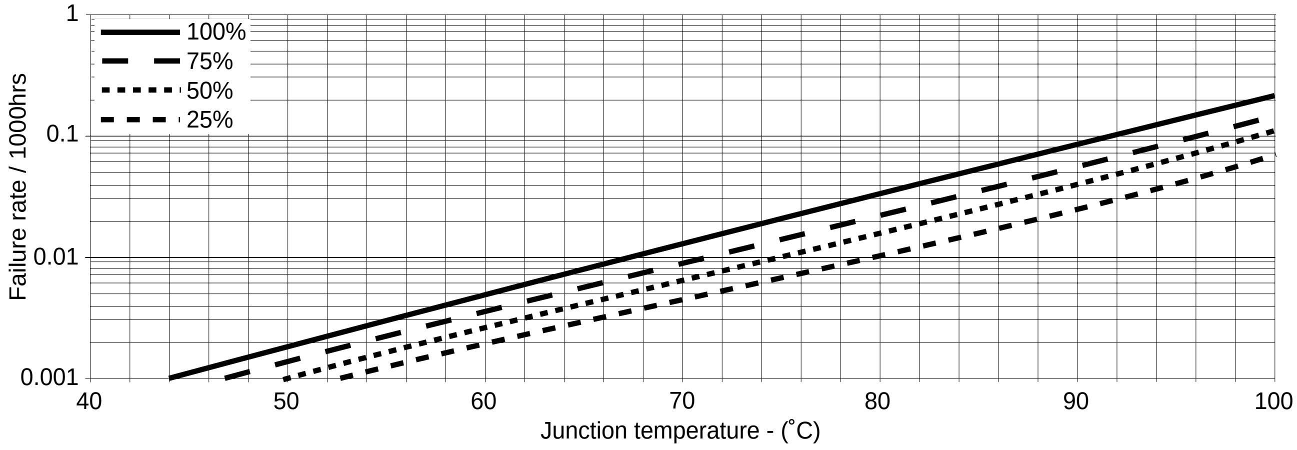

Fig.2 Thyristor failure rate vs applied voltage as a percentage of V_{DRM} (rated) and junction temperature due to ion migration in junction passivation

both reverse and then forward voltage being reapplied. For forward blocking two possible failure modes apply:-

1) Failure to turn-off because of the high turn-off time, t_q value at elevated temperature.

2) Breakover due to high blocking current alone.

The most likely is 1). Variation of t_q with temperature for a range of other conditions must be determined experimentally.

Other important temperatures are:

- Temperatures below $T_{j(max)}$ where ion migration on the silicon surface under the passivation can lead to long term degradation. (See fig.2)
- Continuous T_j permitted before thermal runaway occurs. This is likely to be important only with high leakage thyristors and when very small heatsinks are used.
- Circa 250˚C continuous: Rubber locaters and organic passivation material starts to disintegrate; some annealing-out of electron irradiation.
- Above 600˚C. The metal of the surface contacts starts to penetrate into the silicon causing eventual short circuit. This is probably a factor in di/dt failure.
- 1100 to 1300˚C. This is the temperature reached at non-repetitive di/dt limits. The high local thermal stress causes cracking of the silicon.
- 1415˚C - Melting point of silicon.

Another important temperature limit is the magnitude of temperature excursions (ΔT_j) which relates strongly to the operating life of the device. Slow temperature changes stress the various mechanical parts of the device and cause the movement of one component relative to another due to differential expansion and contraction.

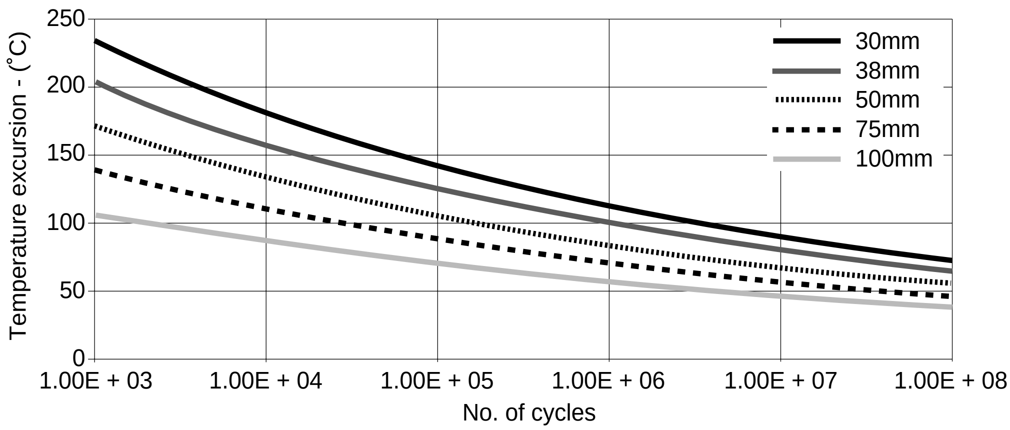

Fig.3 Thermal fatigue life expectancy

Rapid temperature changes associated with highdi/dt can cause micro cracking. It has been shown that, in silicon, micro cracking occurs with ΔT between 300 and 350°C. Somos et al have shown how the value of ΔT relates the expected life time of the device measured in numbers of operations and device diameter. (Fig.3).

Although continuous operation at 250 to 300°C will destroy PN junction characteristics it is possible to operate transiently in this region if allowance is made for reduced device life. Such is the philosophy behind surge current protection when roughly 100 operations up to I_{TSM} values are allowed in the life time of a device. When any overload current wave shape is more complex than a simple sine wave a method of calculating end-of-pulse temperature has to be used. Calculation of steady state T_j takes account of the device case temperature, average current/power loss and steady state thermal resistance. However, for short term overloads it is necessary to include variation of device thermal resistance with time and the device on-state volt drop with temperature. A method of calculating junction temperature using a computer program is described for overloads lasting 1 to about 100ms:

- The information on the overload current is inputted as a series of instantaneous current values with corresponding time points.

- The device transient thermal impedance curve is represented as a polynomial with 5 components, fig.4

$$Z(t) = \sum_{i=1}^{5} A(i).\exp[-t / B(i)]$$

where B = 0.001,0.01,0.1,1.0 and 2 seconds.

Associated with each component is a constant and each device type has its own unique set of 5 constants.

- The variation of on-state voltage with forward current is also represented by a polynomial with 5 components.

$$V(I, T_j) = V\phi(1 + BT \times T_j) + R\phi + I(1 + AL \times T_j) + E\phi(273 + T_j)\,\mathrm{Log}_{10}(i) + 2.3025$$

The curve is determined experimentally using a 10ms half sine pulse which goes to currents which are almost 90% of I_{TSM}. The resultant heating effect is noticeable by the V_F increase on the falling edge of the current pulse. An example of such a "surge loop" is shown in fig.5.

Notice that the surge loop equation includes a temperature term which the normal data sheet V_{TM} curve does not. In other words, the "surge loop" model calculates change in V_{TM} due to junction temperature increase.

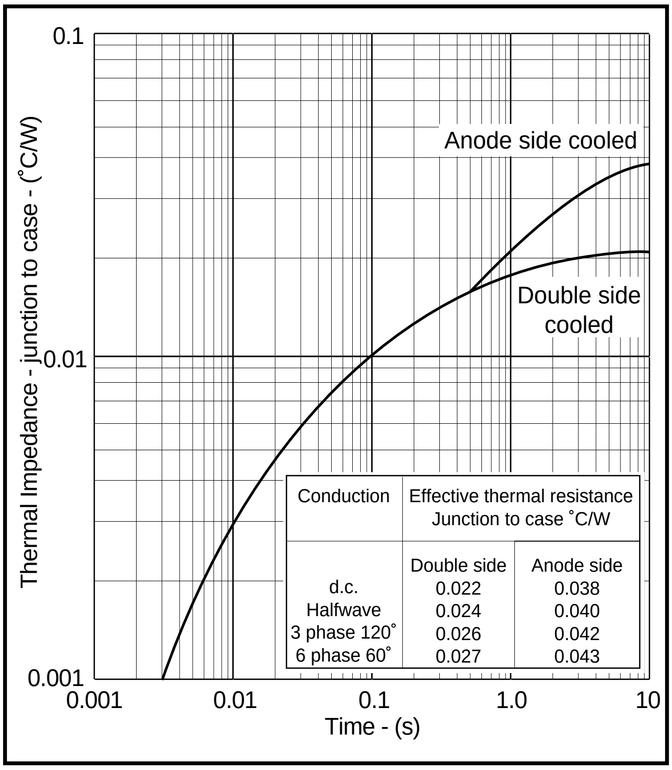

Fig.4 Maximim (limit) transient thermal impedance - junction to case

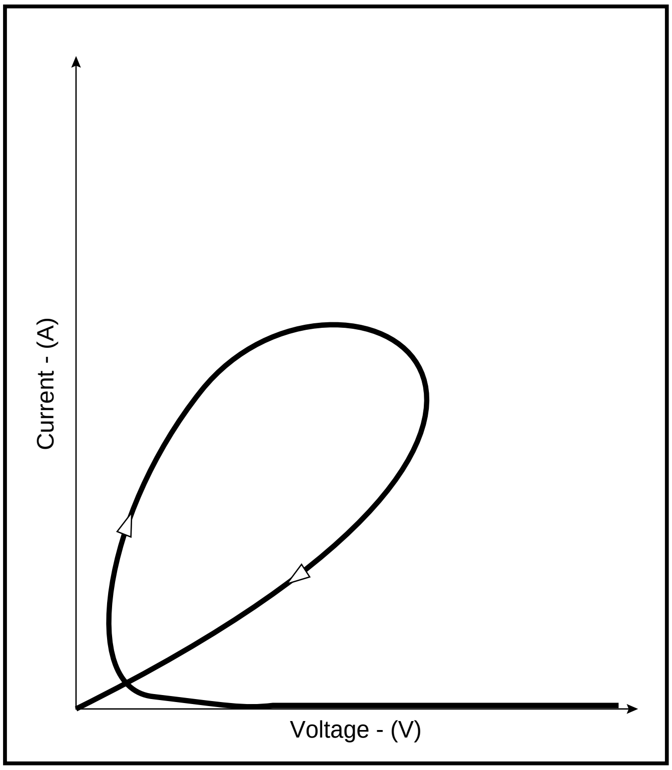

Fig.5 Surge loop

These three input items are then used to calculate instantaneous power and temperature rise at specified time intervals, e.g. 1ms. the procedure using the superposition thereom is as follows:

1. Take the initial T_j at the start of the first 1ms period as T_j (1).
2. Use this in the “surge loop” equation to calculate average power in the first interval. (P1).
3. From the average period power and transient thermal resistance at 1ms calculate temperature rise in the first period and hence starting temperature for second period, $T_j(2)$ where $T_j(2) = T_j(1)$ + T rise (1).
4. Proceed to the second time period and use $T_j(2)$ to calculate appropriate volt drop values and power in this period.
5. Use the average power in period 2 (P2) and the change in thermal resistance between 1ms and 2ms to calculate the rise in the second interval. This then gives the temperature at the end of the second interval, $T_j(3)$.
6. Continue this procedure for as many intervals as necessary.

The procedure is more clearly explained by considering a waveform with 5 intervals.

$$
\begin{aligned}
T_{j(6)} = \; & P1\,[\,Ƶ\,(T_6-T_1) - Ƶ(\,T_6-T_2)\,] \\
& + P2\,[\,Ƶ\,(T_6-T_2) - Ƶ(\,T_6-T_3)\,] \\
& + P3\,[\,Ƶ\,(T_6-T_3) - Ƶ(\,T_6-T_4)\,] \\
& + P4\,[\,Ƶ\,(T_6-T_4) - Ƶ(\,T_6-T_5)\,] \\
& + P5\,[\,Ƶ\,(T_6-T_5)\,]
\end{aligned}
$$

We are using the calculated results as a measure of device survivability so how reliable are the results?

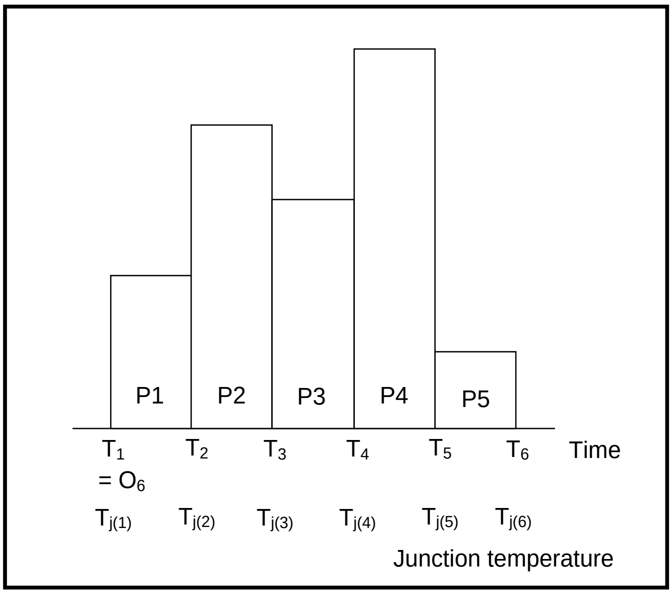

Fig.6

The main assumption is that current flow is uniform across the device area so that temperature is also assumed uniform. This means that current pulses must be wide enough to allow the thyristor to reach full conduction. For small thyristors of a few mm diameter this is easily achievable for pulses of less than 1ms. With larger diameter devices e.g. 30 to 100mm, pulses of several milliseconds are required. For most converter applications this presents no restriction.

Another possible source of error is the potential inaccuracy of the transient thermal impedance curve, particularly at times of 1 to 10ms. It is very difficult to measure this part of the curve so calculation is used. A transmission line model is assumed but since it is difficult to assign accurate values to the various contact thermal resistances between metallic parts conservative values are used. Values depend on surface finishes and clamping forces.

For times longer than about 100ms heat generated at the junction starts to pass into the cooling fin. This is not accounted for in this particular model.

Calculation of temperature rise for short pulses requires more complex 2 and 3 dimensional analysis, possibly involving finite element analysis techniques. Device turn-on behaviour and its dependency on voltage, temperature, di/dt and gate drive has to be taken into account.

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