AN5177

Improved Gate Drive For GTO Series Connections

Application Note

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Using an improved gate drive to ease GTO series connection problems.

INTRODUCTION

There are problems encountered with dynamic voltage sharing of series connected GTOs both at turn-on and turn-off. This application note will deal with the problems associated with turn-off and a further note will address turn-on problems.

Switching high voltages using rectifier diodes or thyristors is routinely done using devices connected in series. With resistor and capacitor networks connected, 100 devices or more can be wired in series.

The basic problem of series connection is to ensure good voltage sharing between devices under both static and dynamic conditions. By using devices selected within defined limits of leakage current and reverse recovery charge, together with correctly sized resistors and capacitors reliable operation is assured.

Unfortunately, series connection of GTOs involves more restraints. For traditional applications such as rail traction where high turn-off currents are important series connection of GTOs has not usually been cost effective. A higher voltage GTO has been the preferred solution. However, this application note shows that even standard design GTOs when used with improved performance gate drive units can be successfully connected in series for certain applications.

In this note, a specific type of application is considered where reverse blocking GTOs are used in series in a current source inverter. In this application, the GTOs are not usually required to turn-off near to their I_{TCM} limits.

THE SERIES CONNECTION PROBLEM

Three modes of operation need to be considered:

1. At GTO turn-on.
2. At GTO turn-off by gate commutation. This is the conventional mode for most GTO applications.
3. At GTO turn-off by anode current reversal i.e. natural commutation. This is similar to diode reverse recovery.

All these operating modes apply to current source inverters. For voltage source inverters turn-off by anode current reversal is not usually relevant.

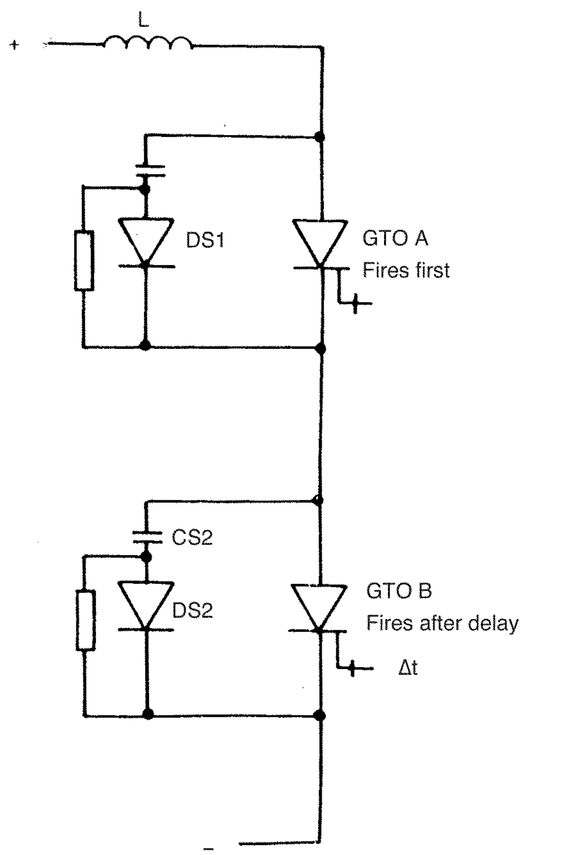

Fig. 1 GTOs in series with snubber networks

TURN-ON

Figure 1 shows two GTOs in series with snubber networks fitted. For simplicity, static sharing parallel resistors are not shown. There will always be a time difference, ΔT, between the GTOs turning on. This time difference is the combination of differences in td and tr of the GTOs, together with the gate drive units propagation time variations.

Figure 2 shows the waveforms at turn-on.

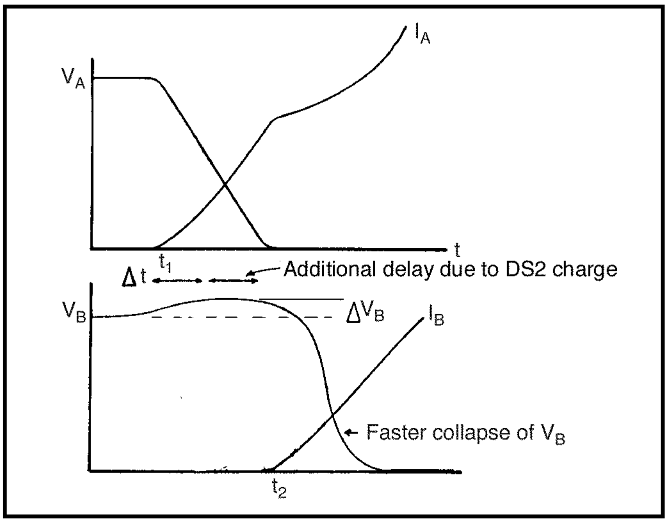

Fig. 2 Turn-on waveforms

TURN-OFF BY GATE COMMUTATION

At turn-off, the voltage mis-sharing, ΔV, is very dependent on Itm, Cs, and Δt_{gs}.

$\Delta V = I_{tm} \cdot \Delta t_{gs}/Cs$

I_{TM}

This is the current being turned-off. This current is relatively low in a current source inverter. By contrast, currents can be very high in a voltage source inverter and this leads to high values of ΔV. Consequently, Cs values must be high to compensate.

Δt_{gs}

This is the difference in storage time between the GTOs in series. Traditionally, GTOs are turned off slowly, typically with dIg/dt = -40A/µs. With this condition, Δt_{gs} values are fairly large. The gate drive unit described achieves turn off current rates of 250A/µs so that tgs and Δt_{gs} are much smaller.

Cs

Snubber capacitor values need to be high to reduce the effect of high Δt_{gs}. It follows that if Δt_{gs} can be reduced so can Cs.

TURN-OFF BY CURRENT REVERSAL

This is the reverse recovery mode, as with a diode and conventional thyristors and is only applicable to reverse blocking GTOs. In this recovery mode the gate drive unit has no effect.

Sharing considerations are as for fast recovery diodes. Thus, to minimise the value of the snubber capacitor the difference between the reverse recovery charge values of the GTOs, (ΔQs) must be kept to a minimum.

SELECTING THE VALUE OF Cs

Cs must be sized for (a) minimising delay time variations at turn-on, (b) conventional GTO gate commutated turn-off and (c) GTO reverse recovery, if appropriate. The requirement for turn-off usually dominates. Clearly, the aim must be to reduce the value of Cs to as low a value as permitted by the application and the GTO specification. Using a gate drive which delivers a higher turn-off gate current rate can help to reduce the required value of Cs.

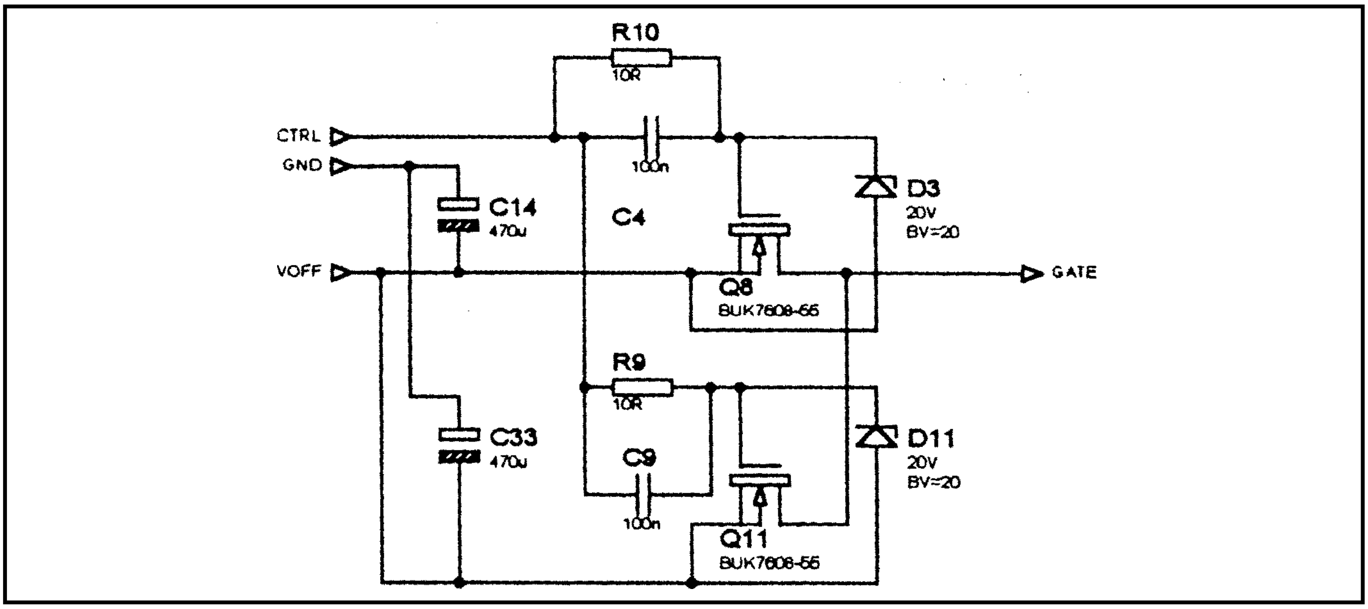

Fig. 3 Simplified version of gdu turn-off section - in reality 10x 470µF capacitors used

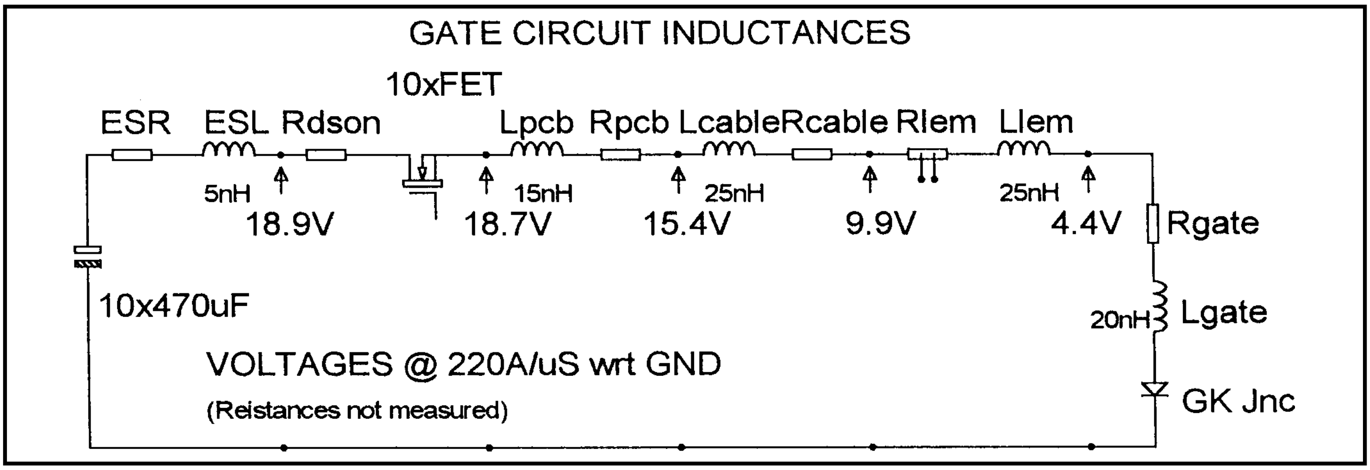

Fig. 4 Loop inductance and dynamic resistance

IMPROVED GATE DRIVE UNIT TURN-OFF PERFORMANCE

A new gate drive unit(GDU) has been designed which gives the GTO improved turn-off performance.

Figure 3 shows a simplified circuit of the turn-off section of the GDU. The turn-off current pulse is achieved by charging a parallel bank of low inductance capacitors to 20 volts and discharging into the GTO gate using MOSFET switches. To achieve a high current and high dIg/dt a low loop inductance is required.

LOOP INDUCTANCE AND DYNAMIC RESISTANCE

The relevant parts of the loop inductance and dynamic resistance are shown in figure 4.

Unfortunately, the physical design of the GTO itself, with its centre gate and gate termination layout, limits the minimum loop inductance which can be achieved. However, careful design of the gate drive PCB and of the interconnecting lead to the GTO housing has resulted in a great reduction in the overall loop inductance. For the GTO type DGT409 a loop inductance of less than 65nH has been achieved. This compares with 500nH for the conventional GDU and lead switching at 40A/µs and around 15nH for the IGCT.

Conventionally, coaxial type cable is used as the gate lead to GTOs but the inductance of a normal cable and its terminations is too high for our application. To minimise the mutual inductance of a connecting lead pair it is necessary to keep the spacing between the forward and return lead as small as possible. A coaxial cable is better than a twisted pair but the strip line is probably the best. Here the conductors are usually thin copper sheets separated by a very thin insulating sheet.

The effective inductance of a conductor is, in part, determined by the operating frequency. The dynamic resistance of a lead is increased at high operating frequencies by the 'skin' effect i.e. the tendency of high frequency currents to flow near the outer surface of a conductor. For this reason, strip line with its high surface area to cross sectional area ratio is an ideal choice for high current pulses with fast rising and falling edges.

PERFORMANCE IMPROVEMENTS IN THE GTO AT GATE TURN-OFF

The performance improvements reported below are for a standard DGT409 which is a reverse blocking GTO type.

In measuring the effects on GTO performance of high dig/dt gate turn off, three areas are of key importance.

1. The effect on turn-off switching loss.
2. The effect on turn-off current rating, Itcm.
3. The effect on storage time.

1. Figure 5 shows the increase in turn-off switching loss with dI_{gt}/dt However, at high dI_{gt}/dt values, above about 50A/µS, the rate of increase is low so the loss penalty for using high dIgt/dt values is small.
2. The effect on I_{tcm} is beneficial. The high dI_{gt}/dt and peak turn-off current ensure that the elements most remote from the gate connection on the edge of the silicon slice receive more gate current than normal. This means that the storage time variations between the elements is much less and sharing of turned off current between elements is much better.

Figure 6 shows the variation of I_{TCM} with Cs for normal and high dI_{GT}/dt.

3. The reduction in storage time, t_{gs}, is very marked between dI_{gt}/dt = -40A/µs and –250A/µs, typically a factor of 6. It follows that as Δt_{gs} also reduces by a factor of 6 then Cs can be reduced by the same factor for the same change in ΔV. Figure 7. However, by the law of diminishing returns further

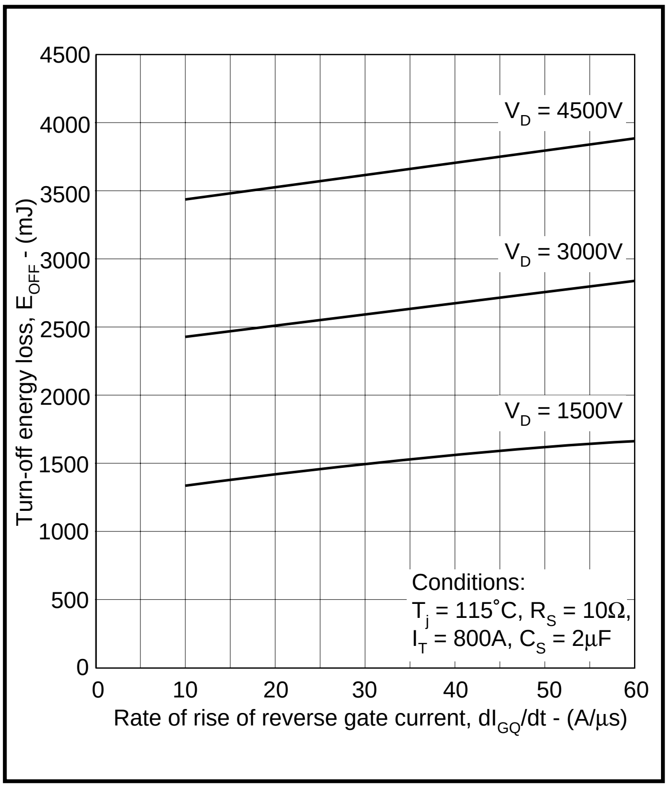

Fig. 5 Turn-off energy vs rate of rise of reverse gate current

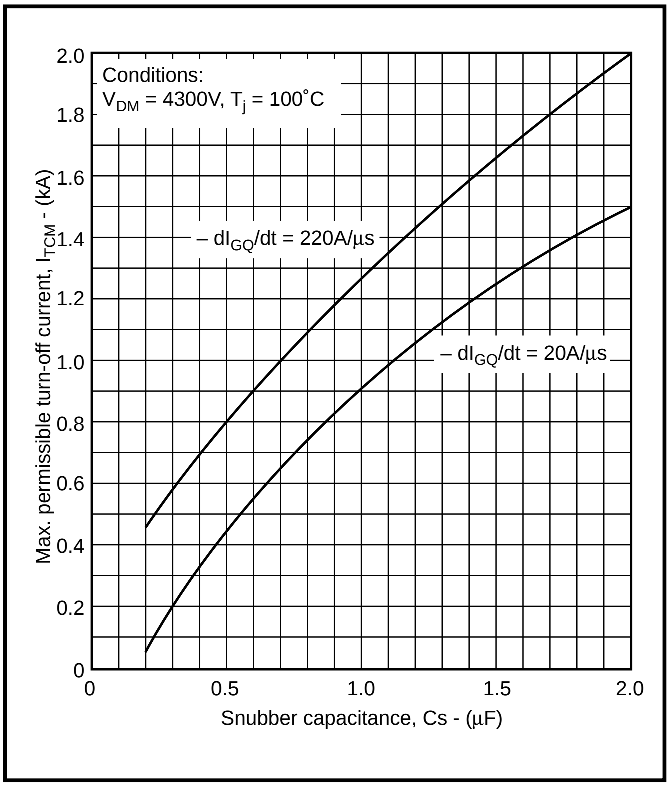

Fig. 6 Max. permissible turn-off current vs snubber capacitance

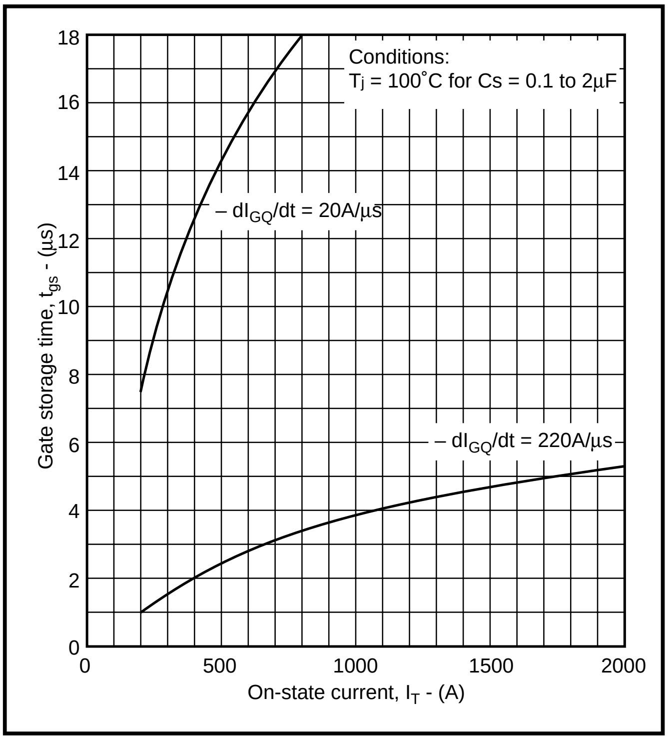

Fig. 7 Gate storgae time vs on-state current

increases in dI_{GT}/dt will have much less effect in further reducing storage time.

4. The reduction in gate turn-off charge Q_{gq} is less marked, typically 40% for a change of dIgt/dt from 40 to 250A/µs. The consequence of this is that the power output requirement of the gate drive unit is reduced by 40%. Again for further increases in dI_{GT}/dt the law of diminishing returns applies.

CONCLUSIONS

Using gate drive circuits with faster rates of rise of gate turn-off current results in higher turn-off current rating, Itcm. Another benefit is the reduction in storage time resulting in smaller sharing capacitors for series connected GTOs. The turn-off power requirements of the gate drive are less for a GTO operating with high rates of rise of turn-off current.

The performance improvements described have been achieved using a relatively low cost gate drive and offer a very cost effective alternative to the IGCT in many applications.

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