

The following information applies to the N- iteration of the MA31750.

Console Mode is an optional feature of MIL-STD-1750 processors in general and is mentioned in MIL-STD-1750. The mode is provided within the MA31750 to allow the system designer to control, monitor and modify internal operation of the processor without having to substantially rewrite system software. This Applications Note describes this mode in detail, giving information on the commands available and the external hardware required to support the Console. This Note updates and corrects the previous issues for the relevant iterations.

OVERVIEW

The processor can operate in one of a number of different modes. One of these is Console mode where the normal MIL-STD-1750 operation is suspended and a special debugging interface is presented instead.

Console mode may be entered by either hardware or software means. When in Console mode the processor receives its instructions from a fixed IO-mapped location. Operands and results (as appropriate) associated with these instructions are passed between system and processor via two other fixed locations in the IO map. Any number of Console commands may be performed before issuing a special command which returns control back to the interrupted 1750 program.

Note that the two interval timers, Timer A and Timer B, are stopped on entry to Console mode, in accordance with MIL-STD-1750.

ENTERING CONSOLE MODE USING CONREQN

Asserting CONREQN low for 2 machine cycles during normal operation will cause the processor to enter Console mode following the completion of the current instruction (but see note on Console inhibit). Whilst CONREQN is low, the device will loop round three machine cycles, one of which will perform a read of the command register (8402₁₆). The command is not executed whilst CONREQN remains low. CONREQN may stay low for as long as required. The user should load the system Console Command register with the desired command before asserting CONREQN high, at which point the requested command will be executed. The flowchart shows the remainder of the command operation. See Table 1 for command information.

ENTERING CONSOLE MODE WITH BPT

If the processor encounters a BPT instruction the processor will enter Console mode (but see note on Console inhibit) and will immediately process the Console command contained in the Command register. It is important, therefore, that the Command register is loaded before any BPT instructions may be encountered. Operation then continues as for CONREQN-initiated commands (see flowchart).

CONSOLE INHIBIT

When CONREQN is asserted low, the CPU checks its internal copy of the configuration register to see if a console is present. If console is entered via the BPT instruction, the CPU reads the system configuration word, hence giving dynamic control over console entry by BPT. If no console is declared in the configuration, CONREQN is ignored and BPT instructions are treated as NOPs.

CONTROLLING THE PROCESSOR IN CONSOLE MODE

When in Console mode the processor communicates with the system console via a number of locations in IO space, as listed below:

Address	Function
8402 ₁₆	Console command input
C000 ₁₆	Data input
4000 ₁₆	Data output
C001 ₁₆	Read Console Status (not used in MA31750)
4001 ₁₆	Clear Console (not used in MA31750)

The user should provide a method of supplying values when these addresses are polled by the processor. A typical approach is to implement three IO-mapped registers which respond to the above addresses and which may be loaded from an external controller or banks of switches.

The required action is communicated to the processor by placing the appropriate command at IO location 8402₁₆ and asserting CONREQN high. If the command takes an operand (such as a value to Write Register) then this should first be placed at location C000₁₆. Following completion of the command, any results are returned via location 4000₁₆. Note that during XIO and Next XIO operations, external read XIO commands execute an extra read of the Data input register. This does not affect the operation in any way. Also note that the IO addresses C001₁₆ and 4001₁₆ are enabled when Console mode is selected, but is not used as part of the Console Mode operation.

Following the execution of the first command, the processor will halt (provided the command is not 'continue') and wait for a further negative edge on CONREQN. The next command to be executed should be set at address 8402₁₆ before the rising edge of CONREQN. Any number of commands may be issued in this way, using CONREQN to control execution and to signal the presence of a new command code to the processor.

LEAVING CONSOLE MODE

To release the MA31750 from Console mode, a 'continue' command should be issued. The instruction pipeline will be refilled with the 1750 instruction immediately following the point at which the Console request or BPT was registered; normal instruction execution then resumes from that point.

SINGLE STEP

Single step operation is also accomplished using a 'continue' command. Once Console mode has been entered, raising CONREQN will cause the processor to execute the command and leave Console mode. If the user reasserts CONREQN low after the 2nd internal cycle after the read and before the 2nd pipe-line pre-fetch, then exactly one 1750 instruction will be executed before the processor returns to Console mode. This allows the processor to step through the 1750 code one instruction at a time.

COMMAND SUMMARY

Table 1 shows a summary of all commands available in Console mode, with a description of their function. Commands should be constructed according to Figure 1. It should be noted that although many of the internal registers are made available in Console mode, attempting to change them may produce predictable but unexpected results. In particular, temporary registers T0, T1 and T9-T11 are used by the Console interface to store operands such as the IC register prior to Console Mode entry.

Command	Function	Code
Continue	Resumes normal MIL-STD-1750 operation. This command is also used for single stepping instructions.	0
Read Register	Places the contents of a specified internal register into the Console Output register (IO address 4000). The register to be accessed is specified as a value placed in the lower 12 bits of the Command register according to Table 2.	1
Write Register	Places the contents of the Console Input register (IO location C000) into a specified internal register. The register to be accessed is specified as a value placed in the lower 12 bits of the Command register according to Table 2.	2
Read and Clear Fault Register	Places the contents of the 1750 Fault register into the Console Output register and then clears the Fault Register.	3
Write Status Word	Copies the contents of the Console Input register to the 1750-defined Status Word register. Note that the A reg is changed to 200E.	4
Read memory	The contents of operand memory space at address A (the contents of the Alternate Address register) are placed in the Console Output register.	5
Write memory	The contents of the Console Input register are placed in operand memory space at address A.	6
Read next memory	The contents of the A register is incremented. The contents of operand memory space at address A are then placed in the Console Output register.	7
Write next memory	The contents of the A register is incremented. The contents of the Console Input register are then placed in operand memory space at address A.	8
XIO	The XIO command specified by the content of the A register is performed using data read from the Console Input register. If the XIO command is illegal the command is ignored. No Status Word Processor State checking is performed.	9
Next XIO	As above, but the command in A is incremented before the XIO is attempted.	A
Disable	Console operation is suspended pending a new Console request or an interrupt. If an interrupt occurs then the Instruction Counter will be restored and normal MIL-STD-1750 operation will be resumed with the interrupt service routine.	B
Reserved	Reserved for internal use by GPS - do not use.	C
Other...	Any other command not described above is ignored and has no action. User should reload Command register with correct value as for a new instruction.	X

Table 1: Console Instructions

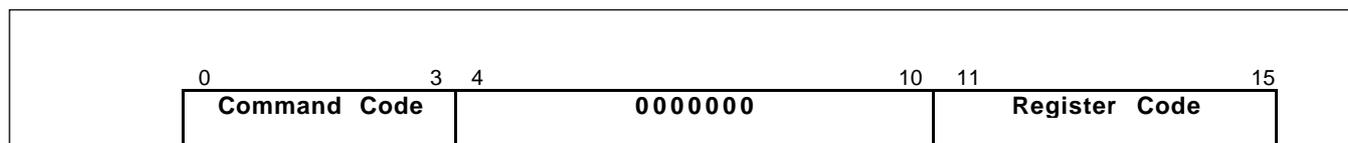


Figure 1: Command Register Format

Register	Register Description	Code (bottom 12 bits)
R0-R15	General purpose register R0-R15	000-00F
T0-T11	Microcode registers T0-T11	010-01B
A	Operand or alternate address register	01C
IC	Instruction Counter (take great care when modifying this value)	01D

Table 2: Register Map

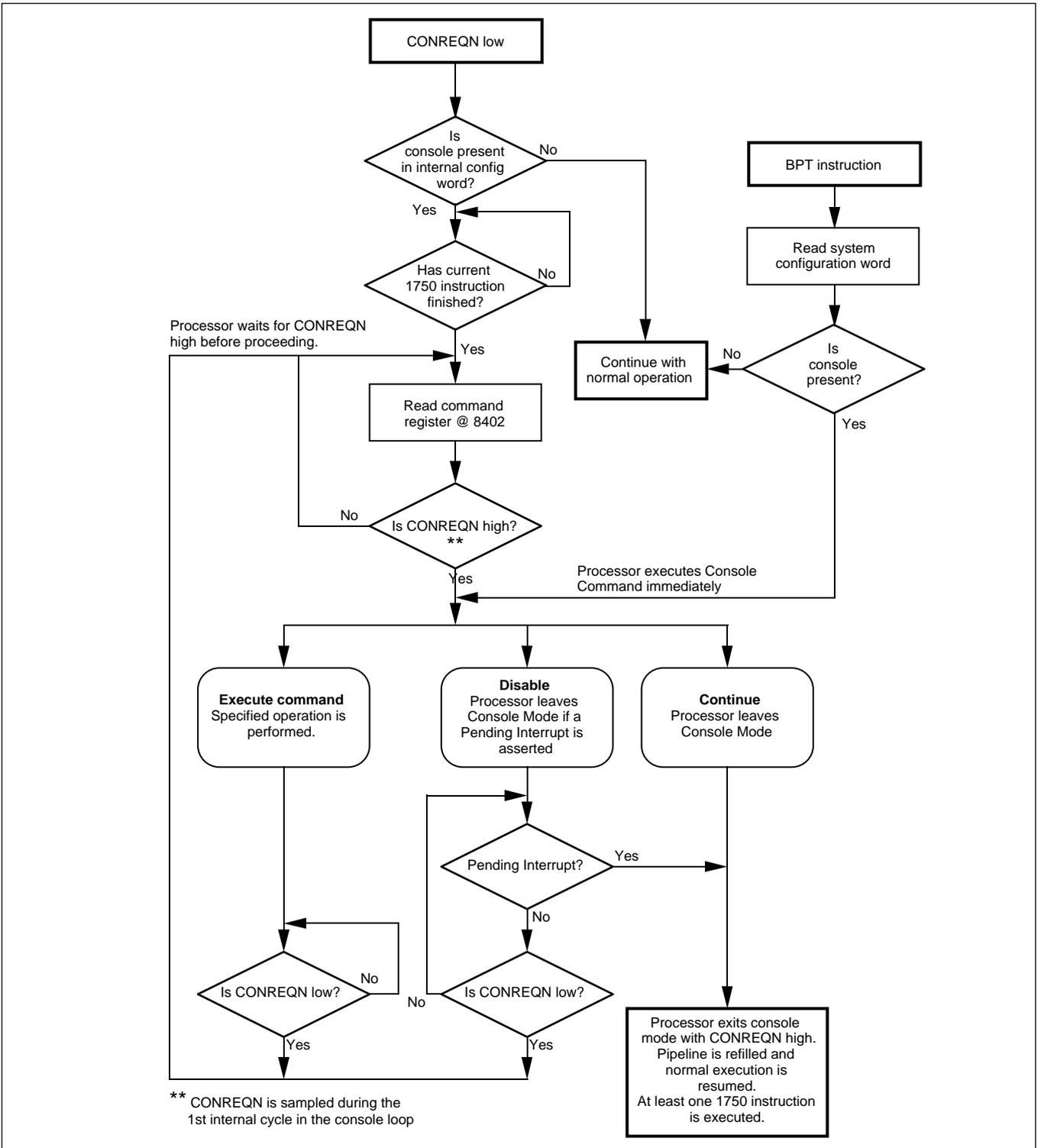


Figure 2: Console Operation Flowchart

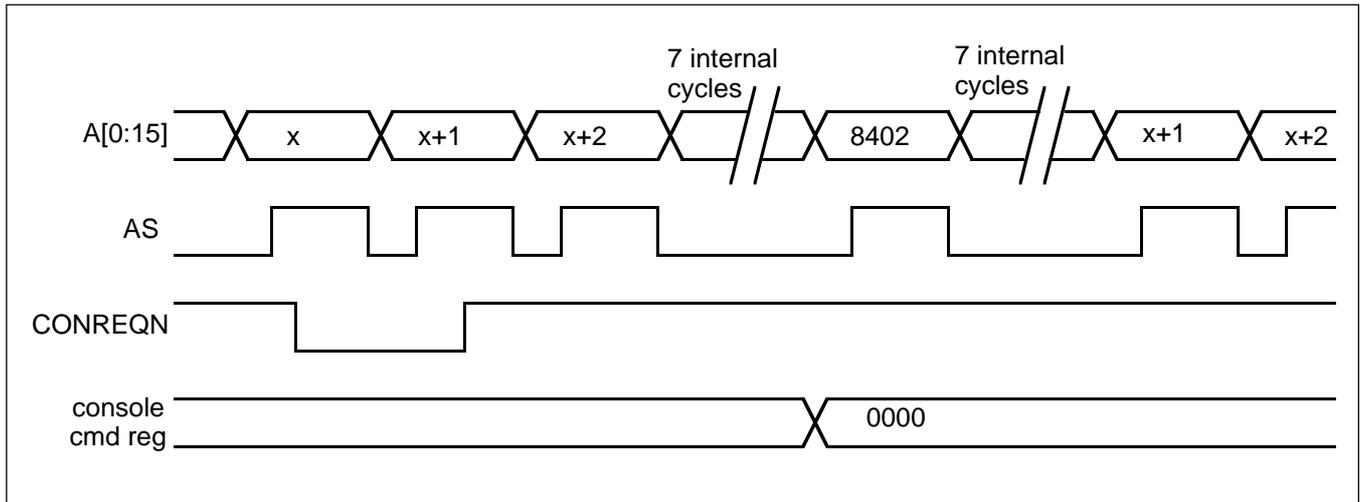


Figure 3: Entering Console Mode

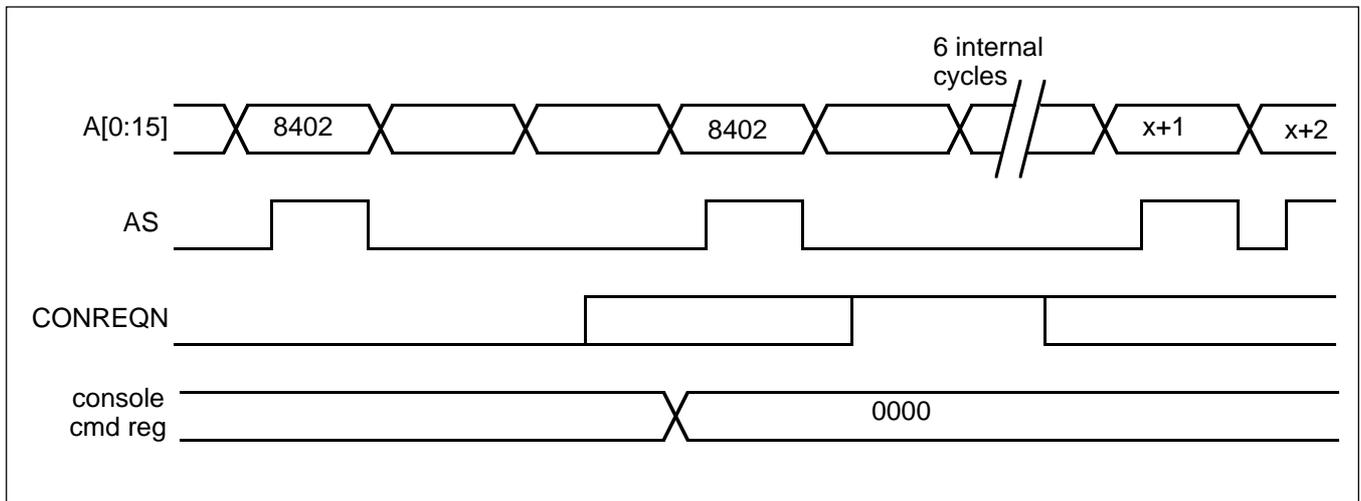


Figure 4: Exiting Console Mode

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.



<http://www.dynexsemi.com>

e-mail: power_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LTD
Doddington Road, Lincoln.
Lincolnshire. LN6 3LF. United Kingdom.
Tel: +44-(0)1522-500500
Fax: +44-(0)1522-500550

CUSTOMER SERVICE
Tel: +44 (0)1522 502753 / 502901. Fax: +44 (0)1522 500020

SALES OFFICES
Benelux, Italy & Switzerland: Tel: +33 (0)1 64 66 42 17. Fax: +33 (0)1 64 66 42 19.
France: Tel: +33 (0)2 47 55 75 52. Fax: +33 (0)2 47 55 75 59.
Germany, Northern Europe, Spain & Rest Of World: Tel: +44 (0)1522 502753 / 502901.
Fax: +44 (0)1522 500020
North America: Tel: (613) 723-7035. Fax: (613) 723-1518. Toll Free: 1.888.33.DYNEX (39639) /
Tel: (949) 733-3005. Fax: (949) 733-2986.

These offices are supported by Representatives and Distributors in many countries world-wide.
© Dynex Semiconductor 2002 TECHNICAL DOCUMENTATION – NOT FOR RESALE. PRODUCED IN UNITED KINGDOM

Datasheet Annotations:

Dynex Semiconductor annotate datasheets in the top right hand corner of the front page, to indicate product status. The annotations are as follows:-

Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification.

This publication is issued to provide information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. The Company reserves the right to alter without prior notice the specification, design or price of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to the Company's conditions of sale, which are available on request.

All brand names and product names used in this publication are trademarks, registered trademarks or trade names of their respective owners.