AN3727

MA31750 - Interrupt Operations

Application Note

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This applications note details the interrupt handling operations of the NMA31750.

INTRODUCTION

The MA31750 has 16 interrupts: 9 of these interrupts are available to the system as external interrupts to the processor, The remaining 7 are internally generated by the MA31750. Interrupts can occur at any time and are latched into the Pending Interrupt register (PI). However, they are not serviced until completion of the currently executing MIL-STD1750 instruction.

MIL-STD-1750 makes provision for interrupt software control via I/O commands. These I/O commands are internally implemented by the MA31750. They provide an enable/ disable facility (without preventing the latching of interrupt requests into the PI) and a means of manipulating the interrupt Mask Register (MK), the PI and the Fault Register (FT) contents.

HARDWARE CONSIDERATIONS

The user interrupts, PWRDN and INT02N-INT15N, can be defined as being edge or level sensitive by the State of bit 4 in the configuration word. If edge sensitivity is selected, an interrupt pulse exceeding the minimum width (specified in the data sheet), appearing at any time in the cycle, will latch an interrupt request. Another interrupt request cannot be detected on that interrupt line until the previous one has cleared.

If level sensitivity is selected, an interrupt will be requested whenever the interrupt signal is active as the PI latches (ie. the same interrupt could be latched multiple times). It is the user's responsibility to deactivate any unwanted external interrupts. INTAKN is asserted low whilst the processor reads the interrupt service pointer (part of the microcoded interrupt service routine). This event may be used to identify and release the interrupt currently being serviced. Figure 1 is a representation of the CPU interrupt latching circuitry.

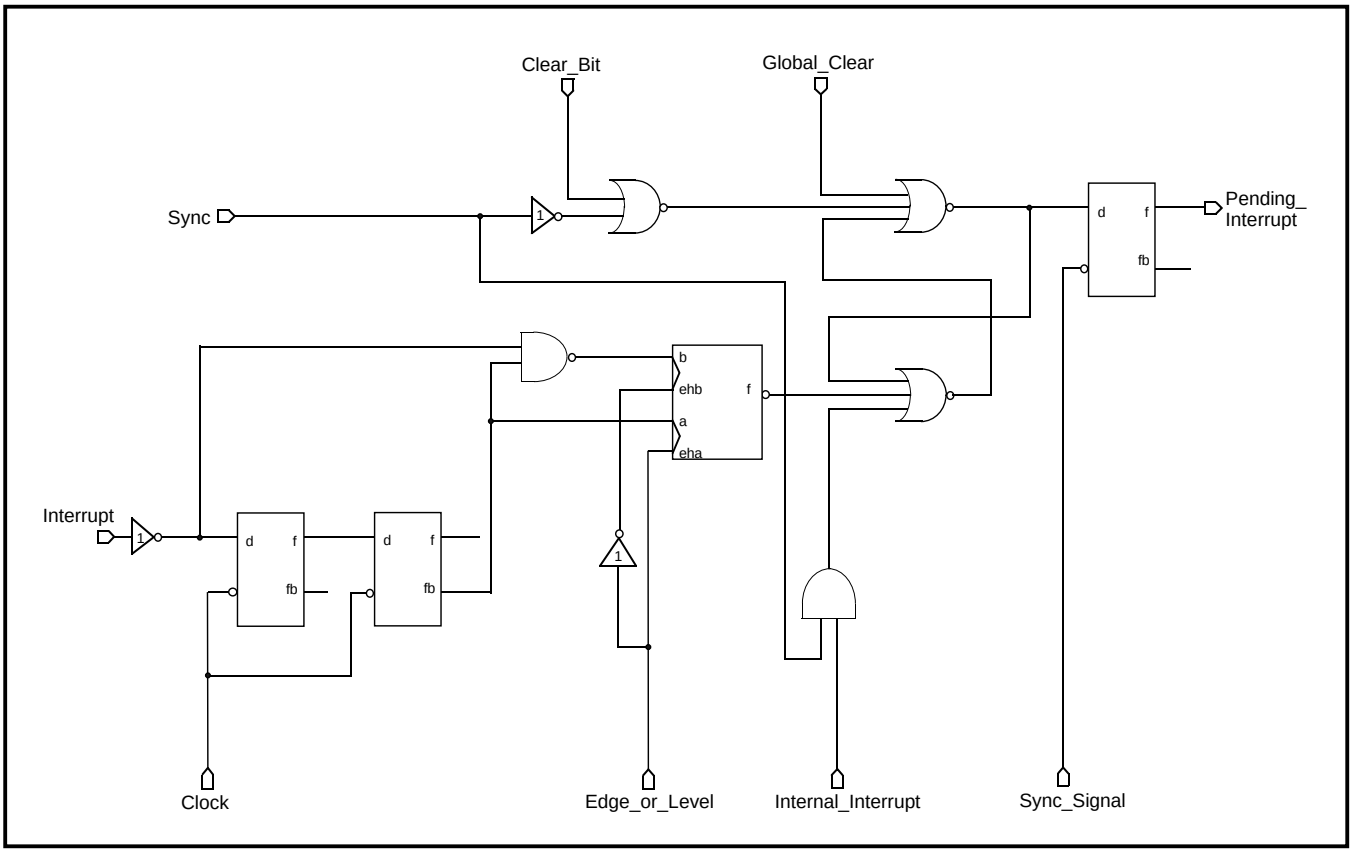

Figure 1: Edge and Level Interrupt Latching Circuit

The internal interrupts are always level sensitive, therefore their latching circuitry does not have the edge detection option. This removes the need for the multiplexer. The cross-coupled NOR gates are also surplus as the asynchronous edge detection has been removed.

As part of the service routine, microcode clears the bit in the PI register asociated with the current interrupt. There are 7 internal interrupts. Interrupt 1, the machine error interrupt signal, differs from the others as it cannot be disabled. It becomes active whenever any of the bits in the Fault Register (FT) are set. There is anti-repeat logic between the FT output and the PI as FT is not cleared when the interrupt is serviced (and re-latching has to be prevented). The FT must be cleared by the user, in the interrupt service routine (by reading and clearing FT) before another machine error can be detected. See Figure 2.

INTERRUPT PROCESSING

Detecting any active interrupt or fault causes a 4 CLK machine cycle to occur on the next machine cycle, (2 early wait states are added). This allows the processor enough time to enter the service routine directly after the currently executing 1750 instruction, even if the interrupt/fault was set as that instruction was completing.

Once an interrupt signal has been set internally, it is ANDed together with the appropriate bit in the Mask Register (MK). If the interrupt has not been masked (only 1-15 can be masked) then the interrupt signal is input to the Priority Encoder. This prioritises the unmasked and enabled interrupts, giving highest priority to the lowest interrupt numbers ie. interrupt 0 is the highest possible priority. The priority encoder outputs a 4-bit interrupt vector and signals to the microcode sequencer that there is an interrupt awaiting processing (service begins when the present 1750 instruction has completed). The vector is read during the interrupt service routine and is used to derive the Linkage Pointer and Service Pointer addresses for the interrupt being processed. Reading the vector also clears the appropriate bit of the Pending Interrupt Register.

INTERRUPT VECTORING

When an interrupt request signal has been received and the processor starts the Microcode Interrupt Service Routine (MISR), the old status of the device has to be stored so that processing can be resumed once the interrupt has been serviced. This old status is stored in a fixed memory location (there is a unique location for each interrupt). The address of this memory location is known as the Linkage Pointer (LP). It references the old mask register (MK), the old status word (SW) and the old instruction counter (IC).

Before execution of the User Interrupt Service Routine (UISR), the context relating to this routine is loaded. The processor loads new values for MK, SW and IC from a three word memory block whose address is held at the Service Pointer (SP) location for that interrupt.

The addresses of the LP and SP for each interrupt are derived from the interrupt vector generated by the priority encoder.

PROCESSING INTERRUPT 5 - BEX

The BEX interrupt is one means of changing the address or processor state of the CPU via software. This allows protected calls to be made to routines in other address states. BEX is called with a number in the range 0-15. This number maps the Instruction Counter onto one of 16 possible new addresses, taken from the memory area pointed to by the SP. Figure 6 shows how the vectoring works for any interrupt.

Note: Most interrupt routines can be called in either of two ways. The interrupt request signal can be activated or the relevant bit in the Pending Interrupt register can be set. However, in 1750B mode, setting bit 5 of the PI (corresponding with BEX) will not generate an interrupt request. In 1750A mode, setting bit 5 in the PI causes BEX 0 to be called.

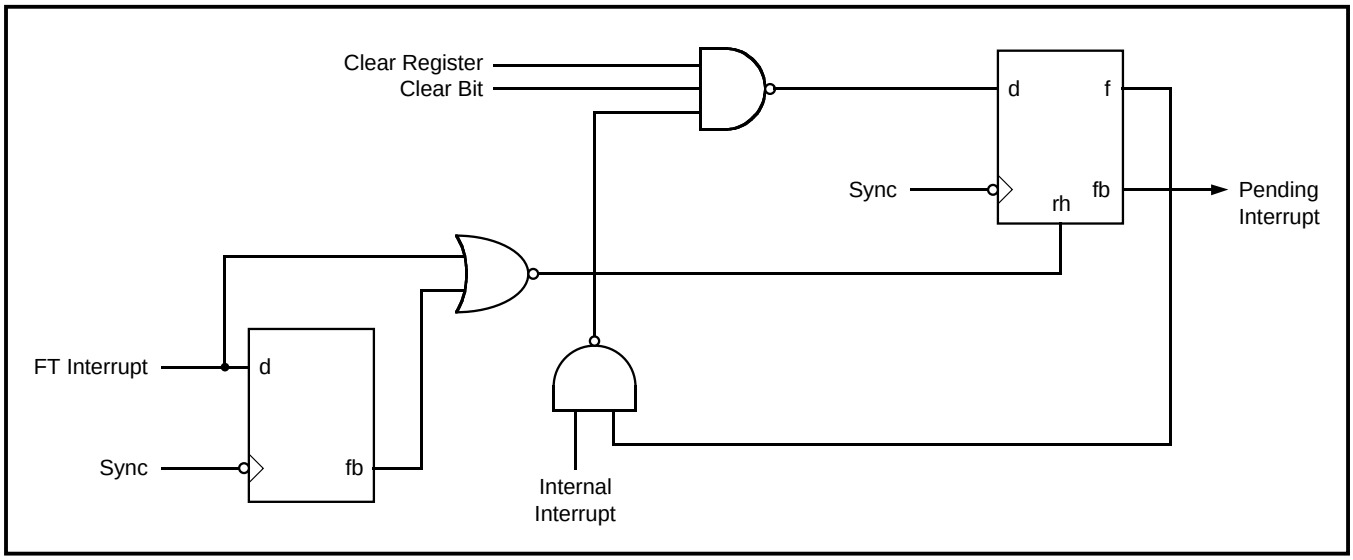

Figure 2: Interrupt 1 Latching Circuitry

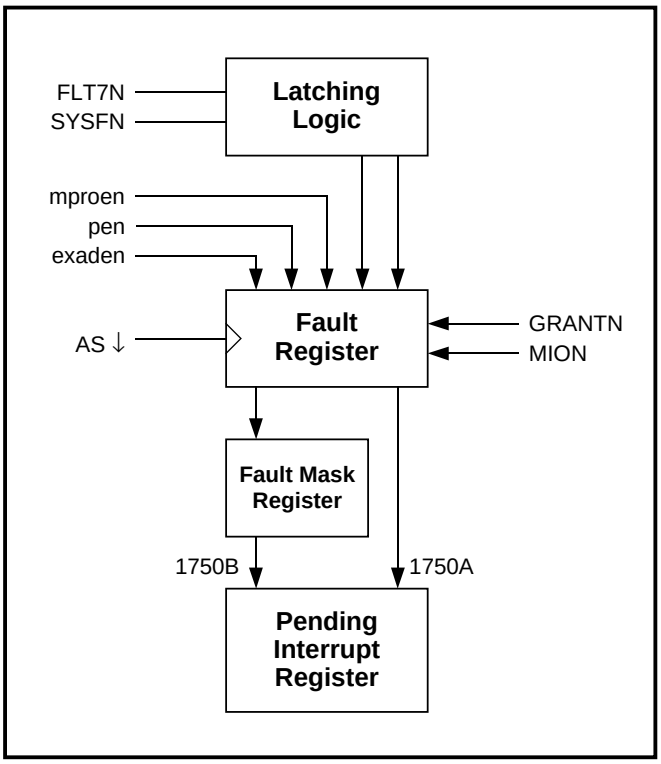

Figure 3: Machine Error Interrupt Capture

MACHINE ERROR FAULTS

Figure 3 shows the latching logic for machine errors. The Fault Register is loaded on the falling edge of the address strobe, AS. This provides synchronicity with the peripherals in the system as they may have control at the time of interrupt generation. The output from the fault register is asynchronously fed into the pending interrupt register (via the fault mask if in 1750B mode). Bit 1 of the PI is set asynchronously as can be seen in Figure 2. This is to ensure that faults are serviced directly after the erroneous instruction. (If the OAS register remains unchanged after initialisation, then abort is enabled. MPROEN and EXADEN will cause the erroneous instruction to be aborted before entering the ME service routine. PEN will cause the next instruction to be aborted if it is an external cycle. The ME is then serviced).

ENDING THE INTERRUPT SERVICE ROUTINE

The software interrupt handling routine is typically ended by using the LST (Load Status) 1750 instruction with the appropriate LP value in (or pointed to by) the address field. LST restores the processor to the state prior to interrupt servicing.

LST is a priviledged instruction, therefore the Processor State (PS) must be set to zero in order for LST to execute. If PS does not equal zero, then the instuction is aborted and the priviledged instruction fault (FT10) is set. This causes a machine error interrupt. If this interrupt is disabled, processing will continue with the 1750 instruction following the aborted LST.

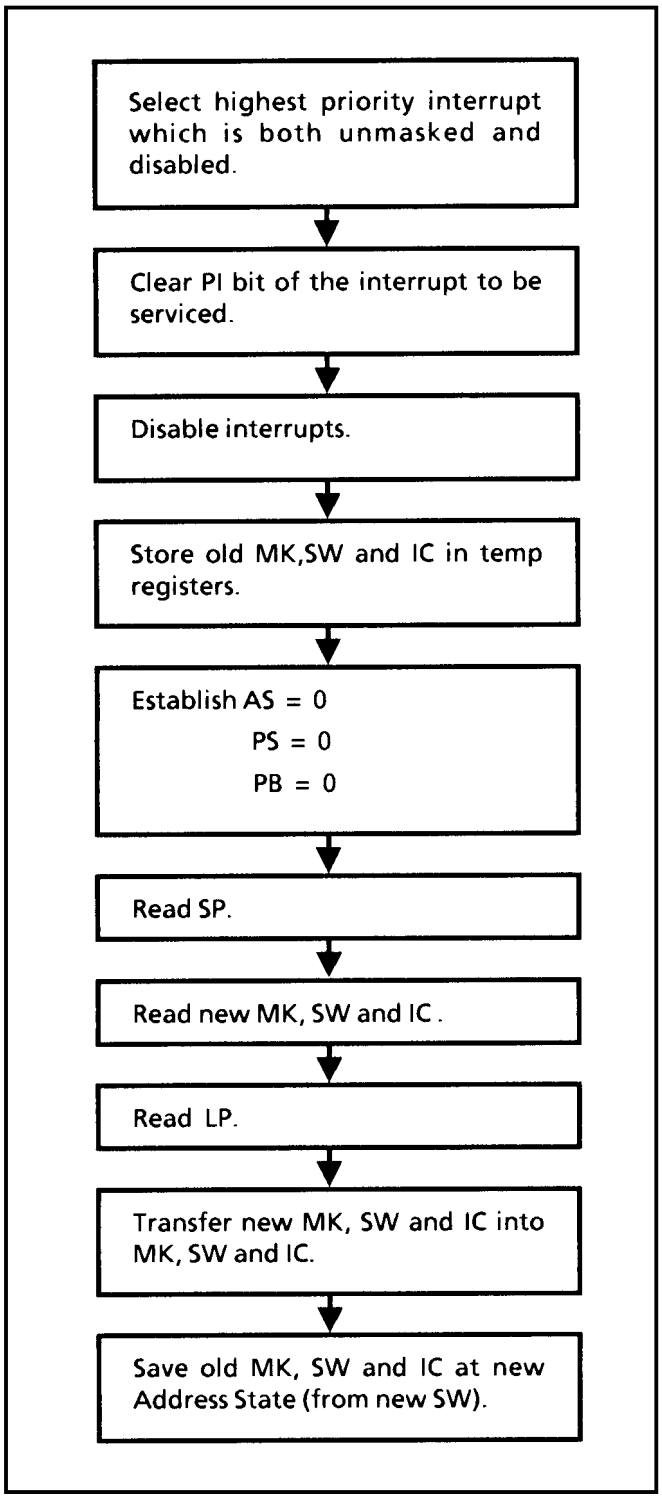

Figure 4: General Description of the Microcode Interrupt Handling Routine

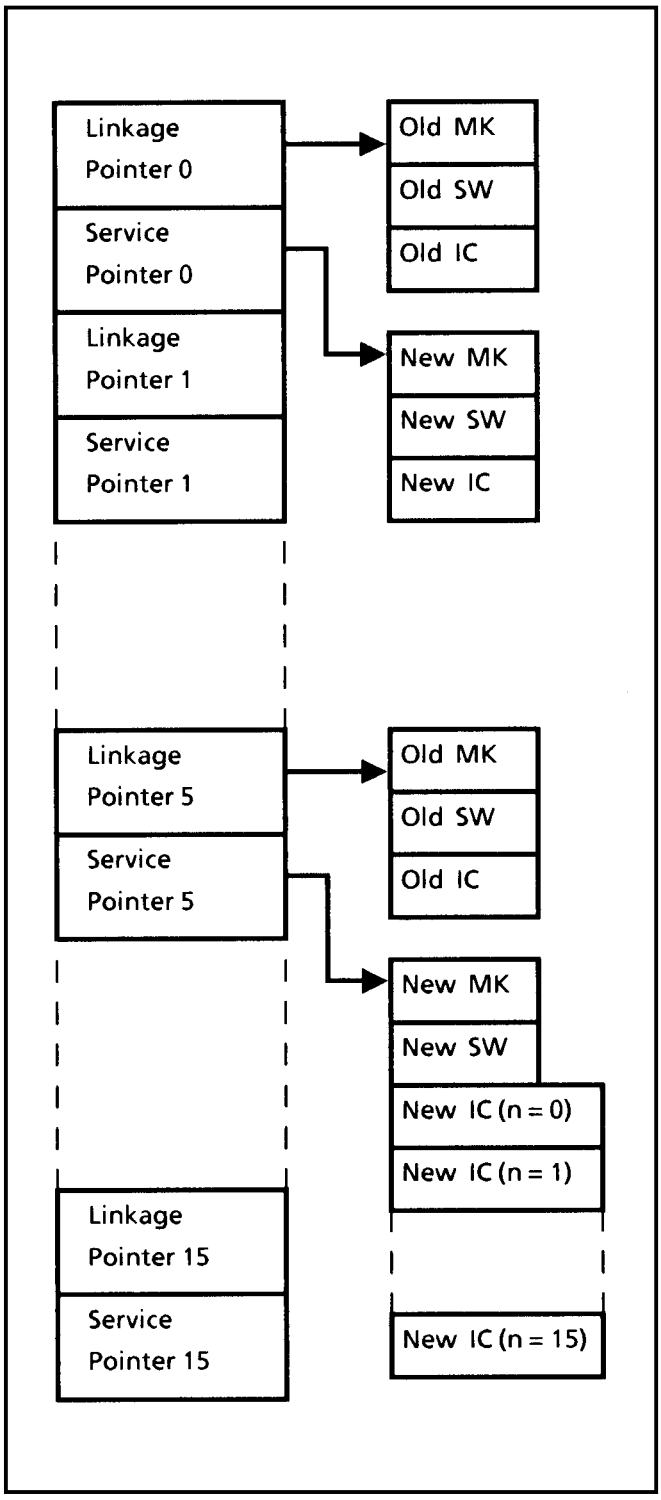

Figure 5: Interrupt Vectoring

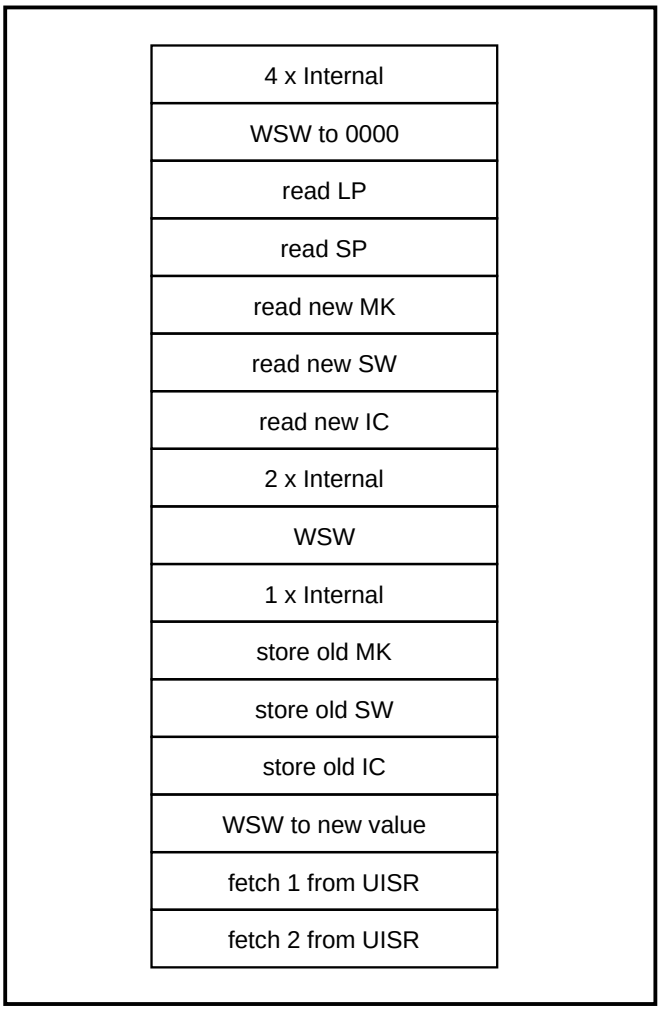

Figure 6: Machine Cycle Description of Interrupt Initialisation

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