1.0 INTRODUCTION

This application note presents a possible solution for a bus arbiter in a multiple-controller MA31750 system. Such an arbiter can be used to arbitrate between the primary MA31750 system and 1 or more other bus masters. These bus masters can be other MA31750 systems, DMA controllers such as the MA31753, or external interfaces.

2.0 PROCESSOR CONSIDERATIONS

When designing a bus arbiter for an NMA31750 system, the following points need to be taken into account:

2.1 LOCKN PULL-UPS

The LOCKN signals should be pulled up because they go tristate when the processor is degranted. Pull-ups are not shown in the arbiters that are described in the next sections, but they must be incorporated.

2.2 PROTECTED CYCLES

The processor internally latches GRANTN on AS falling to ensure that, when GRANTN is removed, the processor continues driving the busses, strobes and control signals until the cycle has completed. However, on the first external cycle after being granted, or the first external cycle after an internal cycle, this latch has not yet been clocked, and there is a danger, when removing GRANTN during these types of cycles, that the processor stops driving whilst strobes are still active. To prevent this from happening, these cycles must be protected from being degranted, or if grant is taken off during a protected cycle, it must be reasserted before AS falling.

2.3 GRANTN TIMING

The processor samples GRANTN on falling CLKOUT, so an arbiter should not allow set-up and hold times to be violated. This can be achieved by latching out the GRANTN signals off the falling edge of CLKOUT of the relevant system. In addition, note that as GRANTN falls to drive the address bus and strobes, the AS can rise off a falling CLK edge. This can erode the address set-up time to AS rising. If this affects the system, then GRANTN must be asserted low to drive the address bus valid and provide the set-up time before the CLK falling edge (and the AS rising edge).

2.4 TCLK TIMING

If the MA31750 is degranted for long periods, a problem can occur: If after degranting the processor, the TCLK falling edge is close to the falling CLK edge at the end of the machine cycle, and then grant is not returned to that system until after another falling edge of TCLK, a cycle may be aborted. (The time-out circuitry is disabled a short time after the end of the degranted cycle. If a TCLK falling edge occurs between the end of the cycle and the disabling of the time-out circuit, then the time-out count remains active. This problem can occur irrespective of the state of DTON.) This can be prevented by synchronising TCLK to CLK to ensure that TCLK only changes during CLKOUT high. This can be achieved by putting TCLK through a D-type that is clocked by CLKOUT from the same system (to be safe, 2 D-types should be used to prevent metastability problems). This is not shown in the next sections.

3.0 2 CHANNEL SYNCHRONOUS BUS ARBITER

The following is an explanation of a bus arbiter that arbitrates between 2 systems, one of which is the default system (system1), but the other having priority over the first (system2). Only the request from system2 is monitored - if it is asserted then grant is given to system2, otherwise grant is given to system1. The lock signals are also monitored to ensure that either system can keep grant during atomic instructions which should not be interrupted. Both systems and the arbiter run off the same clock. An example of such a scheme would be an MA31750 system which gets the bus by default, and a DMA controller which has priority over the processor.

3.1 BUS ARBITRATION LOGIC

The circuit is shown in figure 1. Falling CLKOUT is used to latch in requests and latch out grants to ensure sufficient set-up and hold time of GRANTN to CLKOUT falling (see section 2.3). If the latched request changes state (and LOCKN is inactive), the active grant will be deasserted. Although grant may be taken away immediately, no grant is given until activity on the bus has finished. The signal PRESETN, which prevents a new grant being assigned, is generated from AS or ACTIVE asserted with no grants (ACTIVE comes from the cycle protect logic described in section 3.2). Note that the arbitration logic can be overridden by PROTECT, the other signal from the cycle protect logic (section 3.2), which keeps grant on or reassigns grant to the last system granted.

3.2 CYCLE PROTECT LOGIC

The circuit is shown in figure 2. The cycle protect logic detects activity on the bus by sampling AS on CLKOUT falling. If AS is sampled low, the cycle is inactive and the ACTIVE signal is deasserted (low). ACTIVE high inhibits granting i.e. grants can only be asserted on inactive cycles. This circuit also detects the first external cycle following inactivity on the bus, and from this it generates the signal PROTECT which lasts until AS falling i.e. until the end of the cycle to be protected. This signal is used to prevent degranting of either system if that system is executing the first external cycle. Protecting this cycle from degranting is important for the correct operation of the processor (see section 2.2). Note that the protected cycle can be either the first external cycle after grant has been asserted, or an external cycle following a granted internal cycle.

It can happen that grant is taken off system1 while it is performing internal cycles but just as it is about to perform an external cycle. As soon as AS goes high, the PRESETN signal, which is generated from AS high with no grants, is asserted and prevents granting of system2. At the same time, the PROTECT signal will become asserted and will reassign grant to system1 until the cycle is complete.

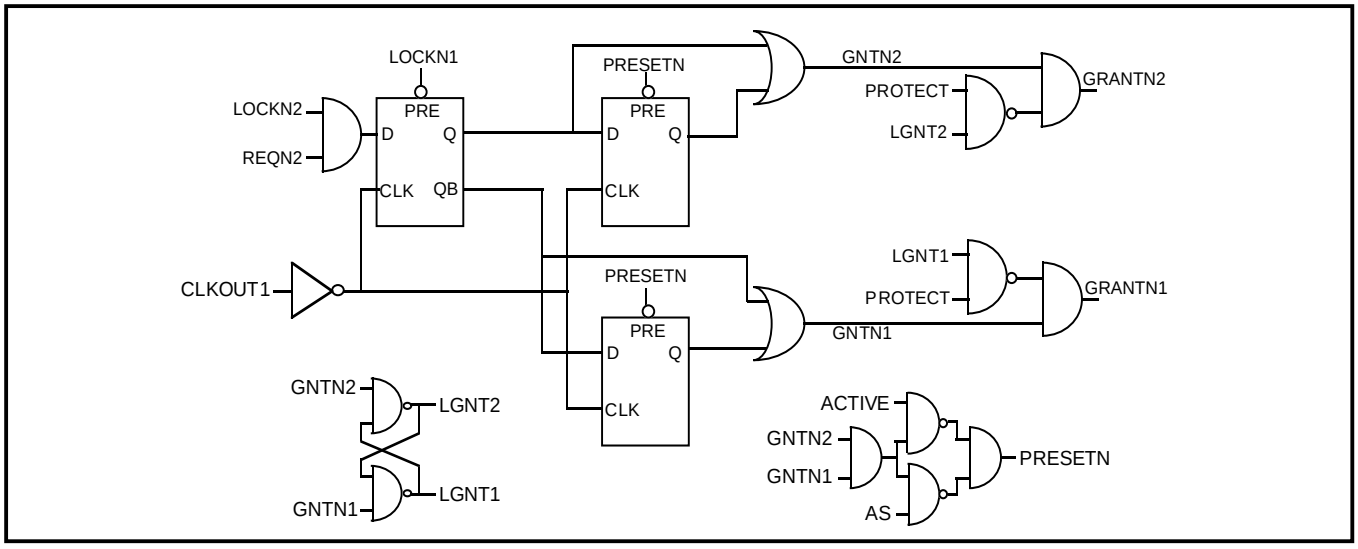

Figure 1: 2 Channel Synchronous Bus Arbitration Logic

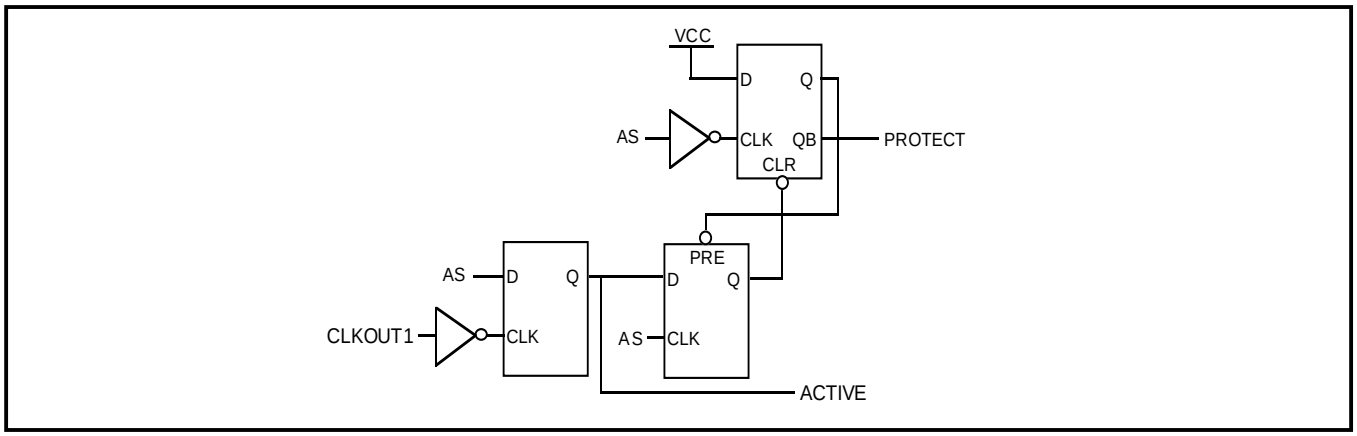

Figure 2: Synchronous Cycle Protect Logic

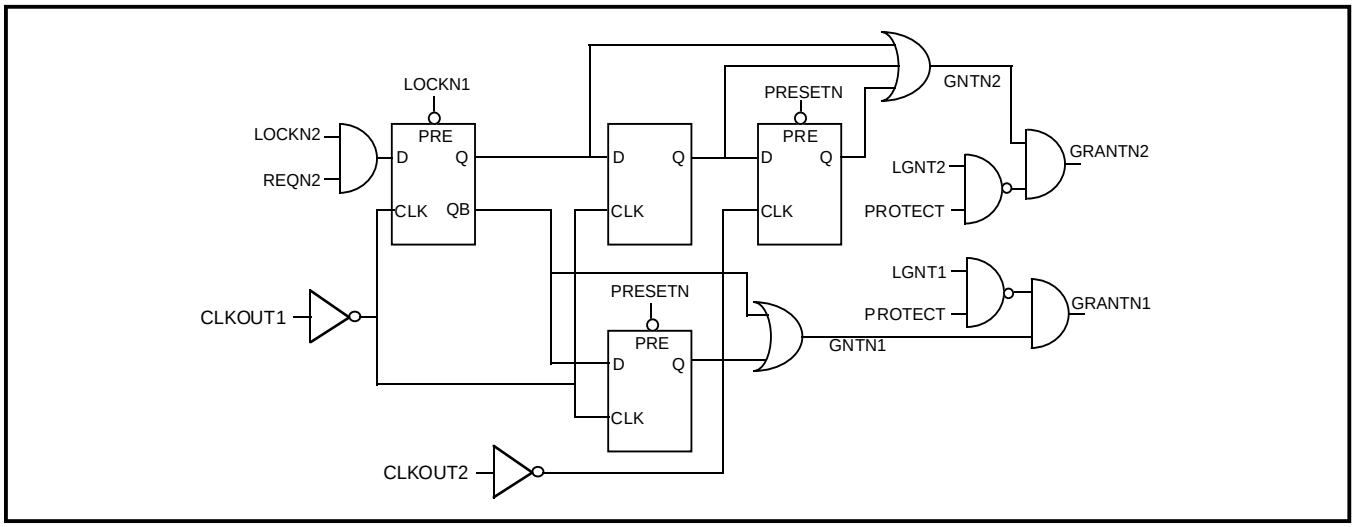

Figure 3: 2 Channel Asynchronous Bus Arbitration Logic

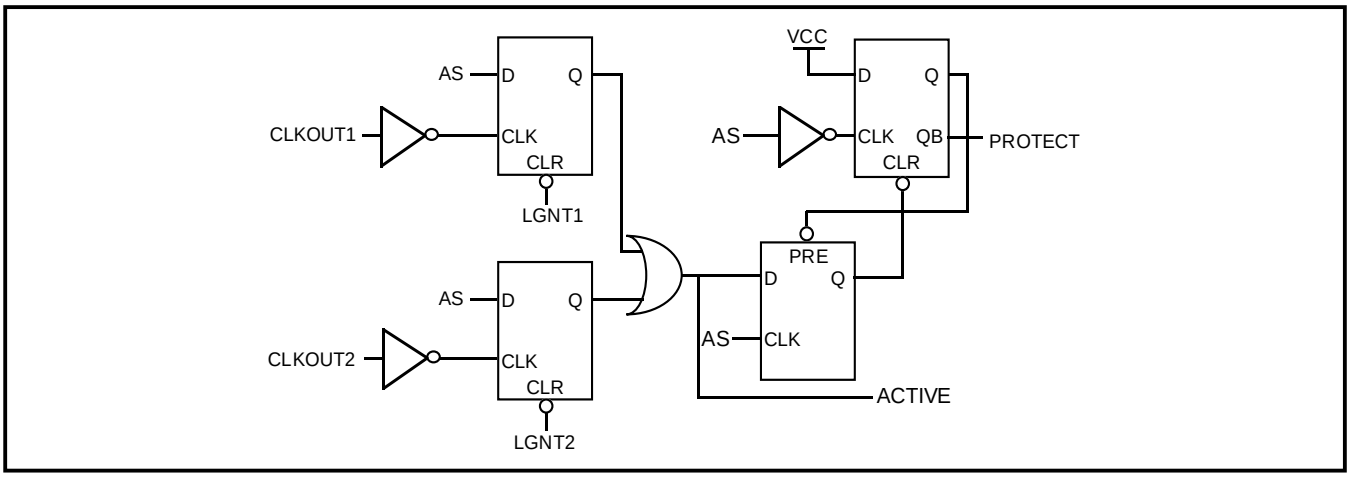

Figure 4: 2 Channel Asysnchronous Cycle Protect Logic

4.0 2 CHANNEL ASYNCHRONOUS BUS ARBITER

This section describes a bus arbiter that is required to arbitrate between 2 systems having separate asynchronous clocks e.g. a processor with an external interface.

4.1 BUS ARBITRATION LOGIC

The bus arbitration logic is shown in figure 3 (the grant latch and preset logic are the same as in figure 1). It is similar to the synchronous case except for the addition of another D-type clocked by CLKOUT2 falling to synchronise GRANTN2 to system2.

4.2 ASYNCHRONOUS CYCLE PROTECT LOGIC

The cycle protect logic is similar to the synchronous case, but now the CLKOUT signals from both system1 and system2 are used to detect activity on the bus. The circuit is shown in figure 4. Note that the latched grant signals LGNT1 and LGNT2 from the arbitration logic are used to select the clock from the system that was last granted.

5.0 3 CHANNEL SYNCHRONOUS BUS ARBITER

This section describes a 3 channel synchronous bus arbiter where system1 is again the default system, system2 has priority over system1 and system3 has priority over both of the other 2 systems (e.g. a processor and 2 DMA controllers).

5.1 BUS ARBITRATION LOGIC

Figure 5 shows the bus arbitration logic which is simply an extension of the 2 channel case.

5.2 CYCLE PROTECT LOGIC

This is exactly the same as for the 2 channel synchronous bus arbiter (figure 2).

6.0 3 CHANNEL ASYNCHRONOUS BUS ARBITER

This section describes a bus arbiter that is required to arbitrate between 3 systems having separate asynchronous clocks e.g. a processor with 2 external interfaces.

6.1 BUS ARBITRATION LOGIC

The bus arbitration logic is shown in figure 6 (the grant latch and the preset logic are the same as in figure 5). It is similar to the synchronous case except for the addition of 2 D-types clocked by CLKOUT2 and CLKOUT3 falling to synchronise GRANTN2 and GRANTN3 to systems 2 and 3 respectively.

6.2 ASYNCHRONOUS CYCLE PROTECT LOGIC

The cycle protect logic is similar to figure 4, but now the CLKOUT signals from all 3 systems are used to detect activity on the bus. The circuit is shown in figure 7.

6.3 WAVEFORMS

Figure 8 shows typical waveforms for the 3 channel asynchronous arbiter described above. The sequence of events is as follows:

1) System 3 executes an external cycle during which it deasserts REQN3.
2) GRANTN3 is deasserted when REQN3 high is latched.
3) ACTIVE goes low followed by GRANTN1 being asserted.
4) System1 executes 2 external cycles followed by an internal cycle, REQN2 is asserted during the internal cycle.
5) REQN2 low is latched and GRANTN1 is deasserted.
6) System 1 executes another external cycle so PROTECT is asserted and GRANTN1 reasserted.
7) GRANTN1 is deasserted at the end of this cycle.
8) When ACTIVE has gone low, GRANTN2 is asserted.
9) System 2 starts executing external cycles, starting with a protected cycle.

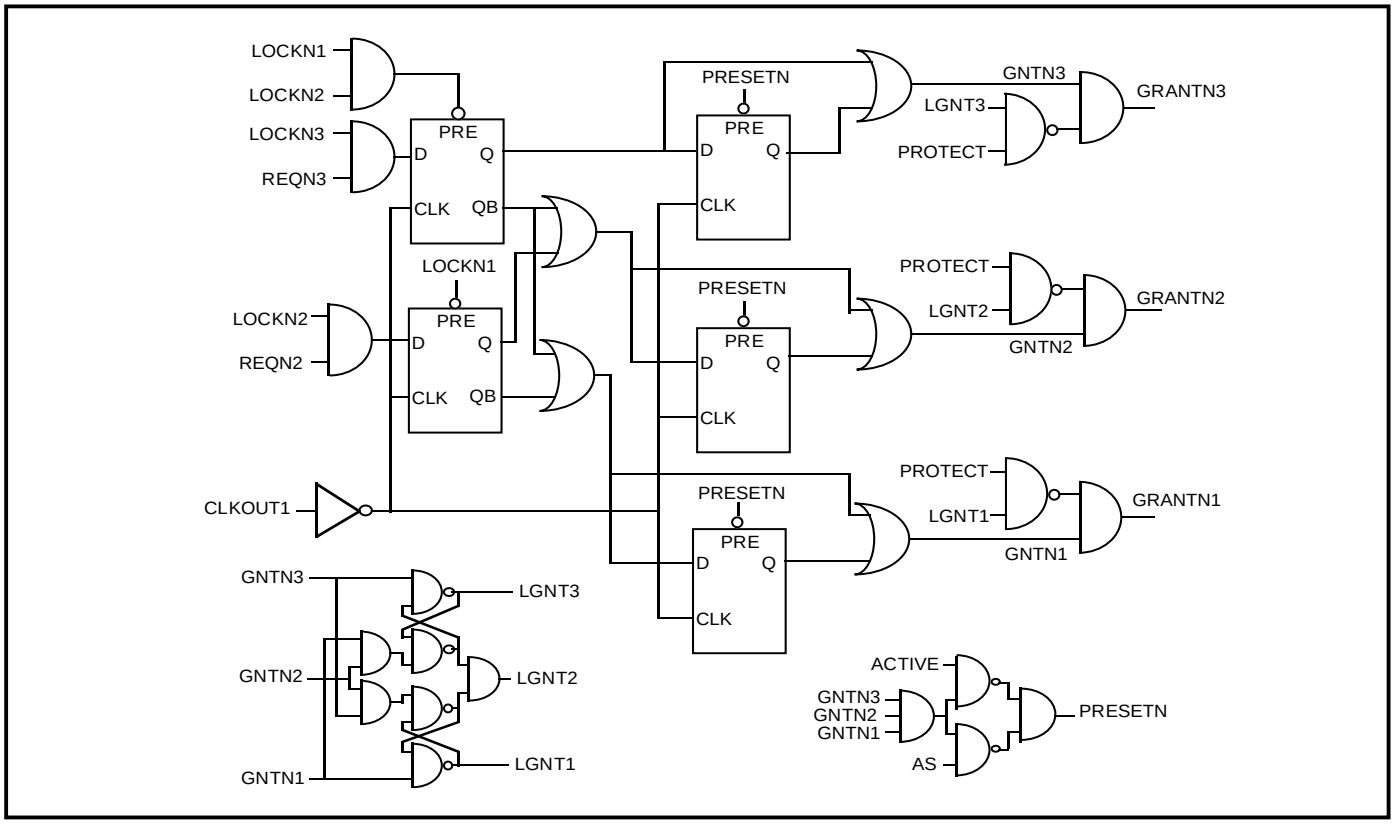

Figure 5: 3 Channel Synchronous Bus Arbitration Logic

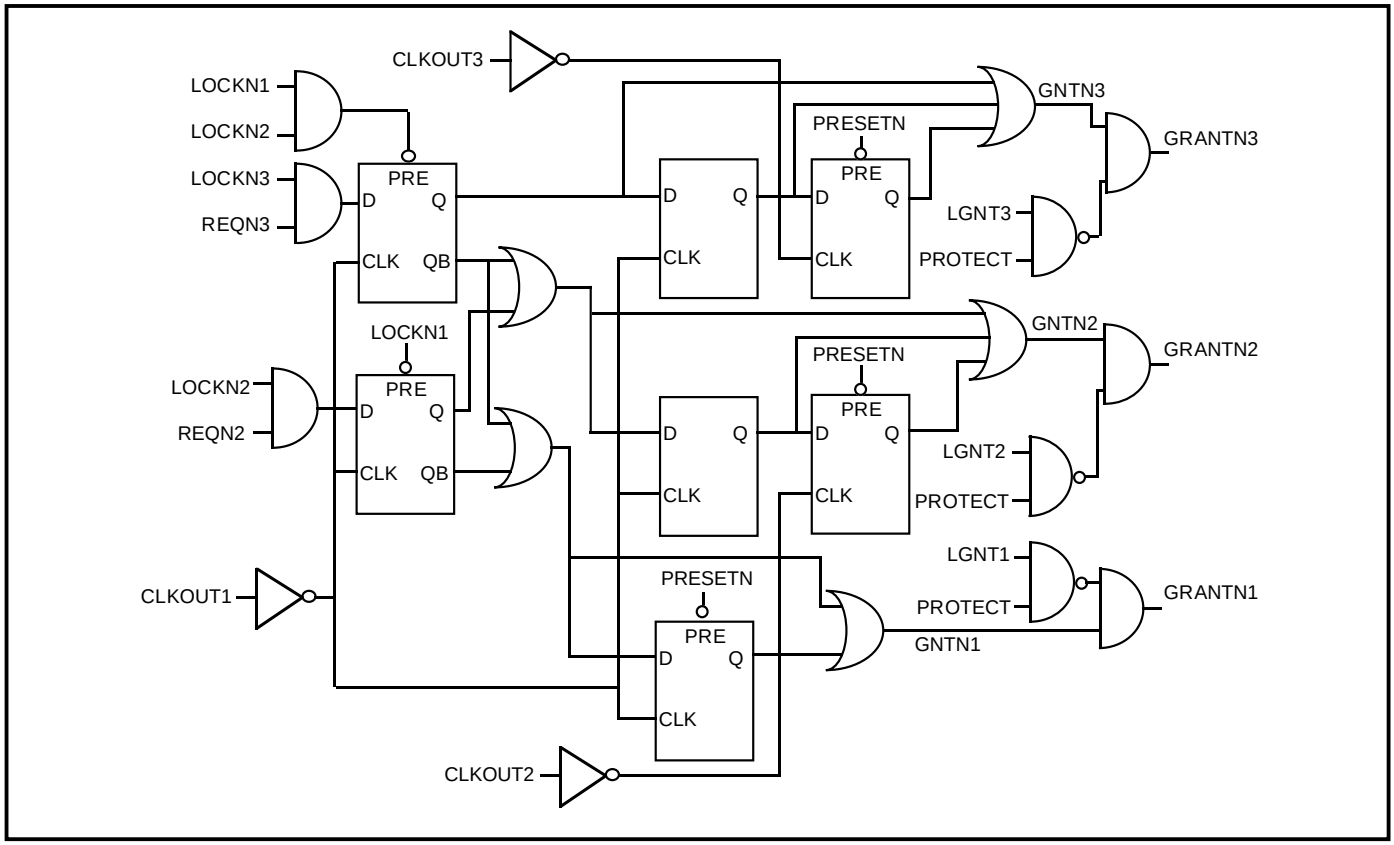

Figure 6: 3 Channel Asynchronous Bus Arbitration Logic

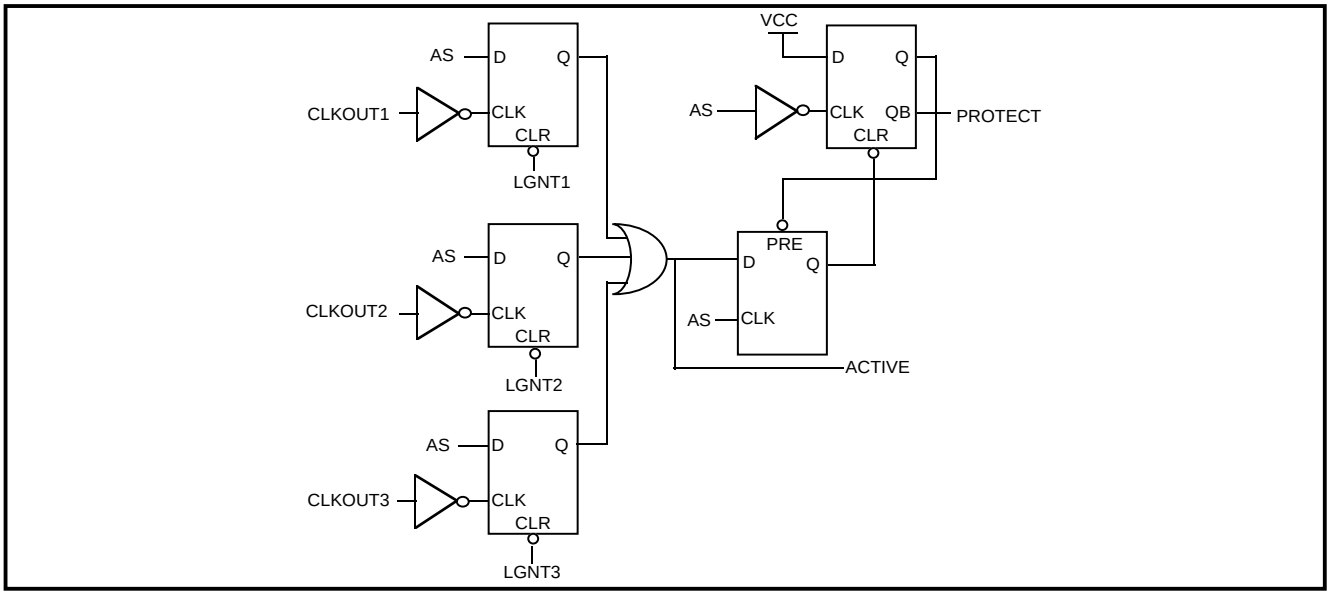

Figure 7: 3 Channel Asynchronous Cycle Protect Logic

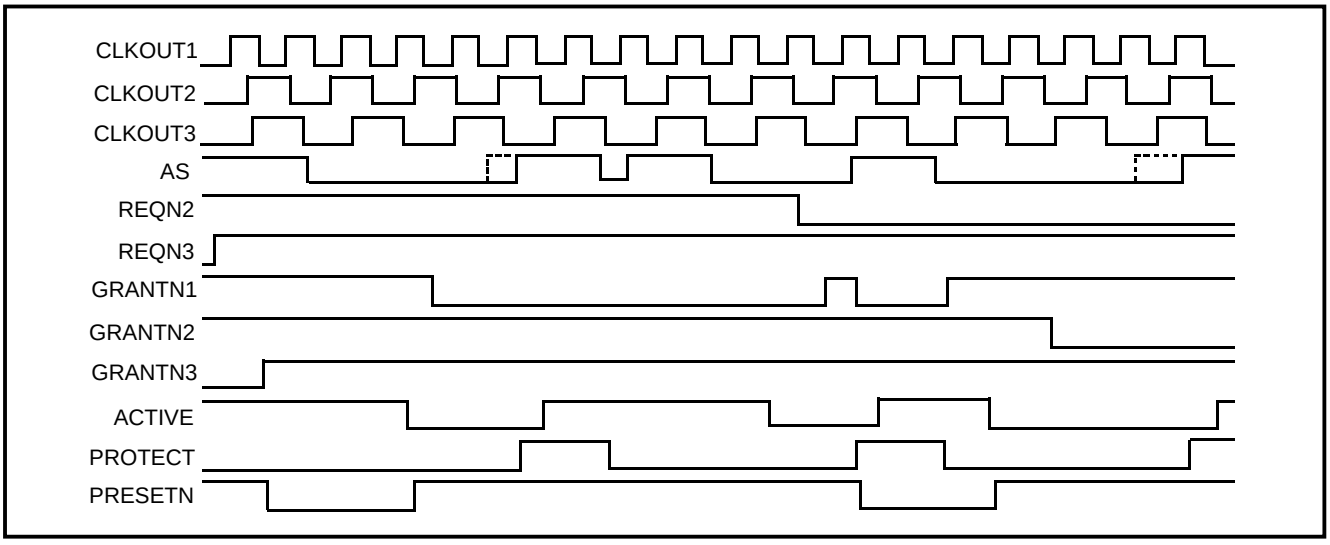

Figure 8: Typical Waveforms for 2 Channel Asynchronous Arbiter

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