

FEATURES

- Double Side Cooling
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- High Surge Current Capability
- Turn-off Capability Allows Reduction In Equipment Size And Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements

APPLICATIONS

- Variable speed A.C. motor drive inverters (VSD-AC)
- Uninterruptable Power Supplies
- High Voltage Converters
- Choppers
- Welding
- Induction Heating
- DC/DC Converters

KEY PARAMETERS

I_{TCM}	700A
V_{DRM}	1800V
$I_{T(AV)}$	240A
dV_D/dt	500V/μs
di_T/dt	500A/μs

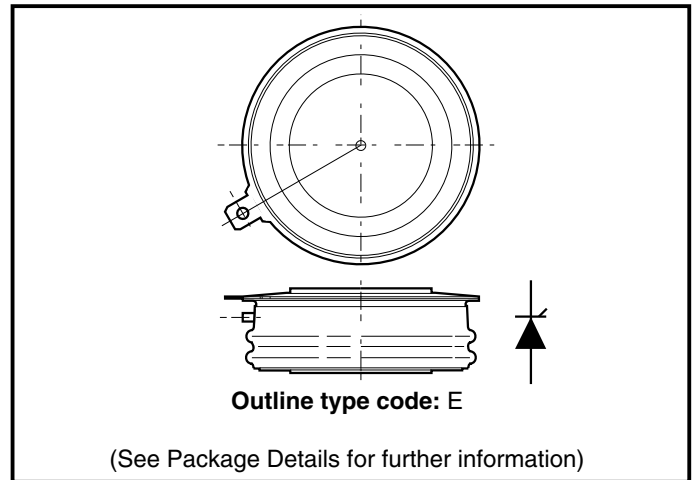


Fig. 1 Package outline

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V	Conditions
DGT305SE18	1800	16	$T_{vj} = 125^{\circ}C$, $I_{DM} = 50mA$, $I_{RRM} = 50mA$, $V_{RG} = 2V$

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	$V_D = 67\%V_{DRM}$, $T_j = 125^{\circ}C$, $di_{GD}/dt = 15A/\mu s$, $C_s = 1.5\mu F$	700	A
$I_{T(AV)}$	Mean on-state current	$T_{HS} = 80^{\circ}C$. Double side cooled. Half sine 50Hz.	240	A
$I_{T(RMS)}$	RMS on-state current	$T_{HS} = 80^{\circ}C$. Double side cooled. Half sine 50Hz.	373	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine. $T_j = 125^\circ\text{C}$	4.0	kA
I^2t	I^2t for fusing	10ms half sine. $T_j = 125^\circ\text{C}$	80000	A^2s
di_T/dt	Critical rate of rise of on-state current	$V_D = 67\% V_{DRM}$, $I_T = 700\text{A}$, $T_j = 125^\circ\text{C}$, $I_{FG} > 20\text{A}$, Rise time $< 1.0\mu\text{s}$	500	$\text{A}/\mu\text{s}$
dV_D/dt	Rate of rise of off-state voltage	To 80% V_{DRM} ; $R_{GK} \leq 1.5\Omega$, $T_j = 125^\circ\text{C}$	500	$\text{V}/\mu\text{s}$
V_{DP}	Peak forward transient voltage during current fall time	$V_D = 67\% V_{DRM}$, $I_T = 700\text{A}$, $T_j = 125^\circ\text{C}$, $di_{GQ}/dt = 15\text{A}/\mu\text{s}$, $C_s = 1.5\mu\text{F}$	400	V

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		-	50	A
$P_{FG(AV)}$	Average forward gate power		-	10	W
P_{RGM}	Peak reverse gate power		-	6	kW
di_{GQ}/dt	Rate of rise of reverse gate current		10	50	$\text{A}/\mu\text{s}$
$t_{ON(min)}$	Minimum permissible on time		20	-	μs
$t_{OFF(min)}$	Minimum permissible off time		40	-	μs

THERMAL RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units	
$R_{th(j-hs)}$	DC thermal resistance - junction to heatsink surface	Double side cooled	-	0.075	$^\circ\text{C}/\text{W}$	
		Anode side cooled	-	0.12	$^\circ\text{C}/\text{W}$	
		Cathode side cooled	-	0.20	$^\circ\text{C}/\text{W}$	
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 5.5kN With mounting compound	per contact	-	0.018	$^\circ\text{C}/\text{W}$
T_{vj}	Virtual junction temperature		-	125	$^\circ\text{C}$	
T_{OP}/T_{stg}	Operating junction/storage temperature range		-40	125	$^\circ\text{C}$	
-	Clamping force		5.0	6.0	kN	

CHARACTERISTICS

T_j = 125°C unless stated otherwise					
Symbol	Parameter	Conditions	Min.	Max.	Units
V _{TM}	On-state voltage	At 600A peak, I _{G(ON)} = 2A d.c.	-	2.5	V
I _{DM}	Peak off-state current	At V _{DRM} , V _{RG} = 2V	-	50	mA
I _{RRM}	Peak reverse current	At V _{RRM}	-	50	mA
V _{GT}	Gate trigger voltage	V _D = 24V, I _T = 100A, T _j = 25°C	-	0.75	V
I _{GT}	Gate trigger current	V _D = 24V, I _T = 100A, T _j = 25°C	-	1.2	A
I _{RGM}	Reverse gate cathode current	V _{RGM} = 16V, No gate/cathode resistor	-	50	mA
E _{ON}	Turn-on energy	V _D = 1200V, I _T = 600A,	-	160	mJ
t _d	Delay time	I _{FG} = 20A, rise time < 1.0μs	-	1.1	μs
t _r	Rise time	R _L = (Residual inductance 2.75μH)	-	2.5	μs
E _{OFF}	Turn-off energy	I _T = 600A, V _D = 1200V, Snubber Cap Cs = 1.5μF, di _{GQ} /dt = 15A/μs R _L = (Residual inductance 2.75μH)	-	550	mJ
t _{tail}	Tail time		-	30	μs
t _{gs}	Storage time		-	12	μs
t _{gf}	Fall time		-	1.5	μs
t _{gq}	Gate controlled turn-off time		-	13.5	μs
Q _{GQ}	Turn-off gate charge		-	900	μC
Q _{GQT}	Total turn-off gate charge		-	1800	μC

CURVES

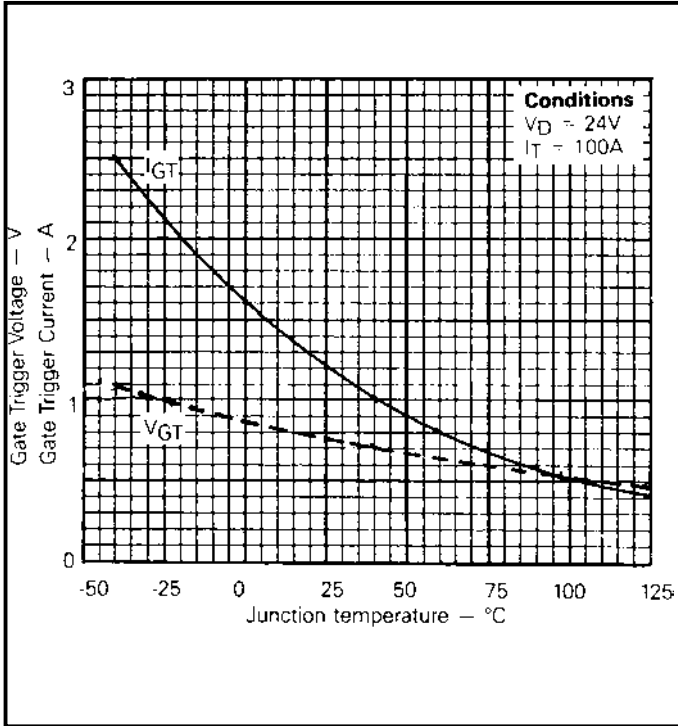


Fig.2 Gate characteristics

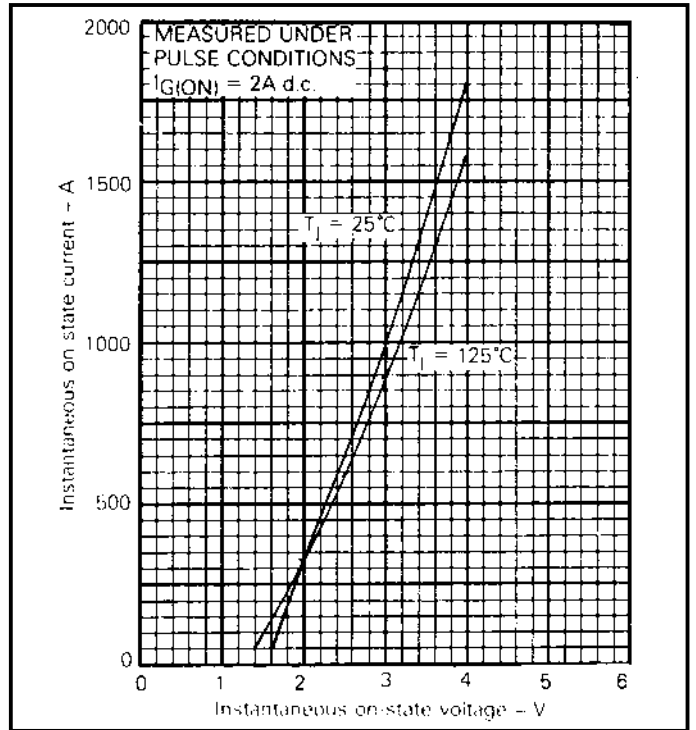


Fig.3 Maximum (limit) on-state characteristics

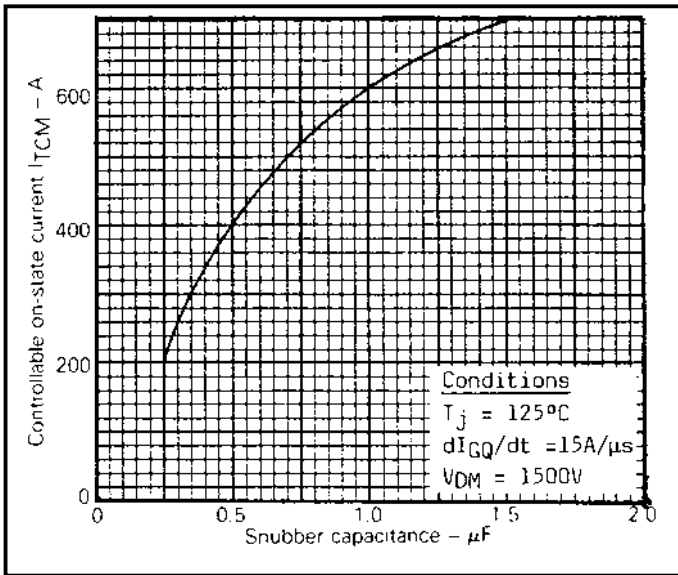


Fig.4 Dependence of I_{TCM} on C_s

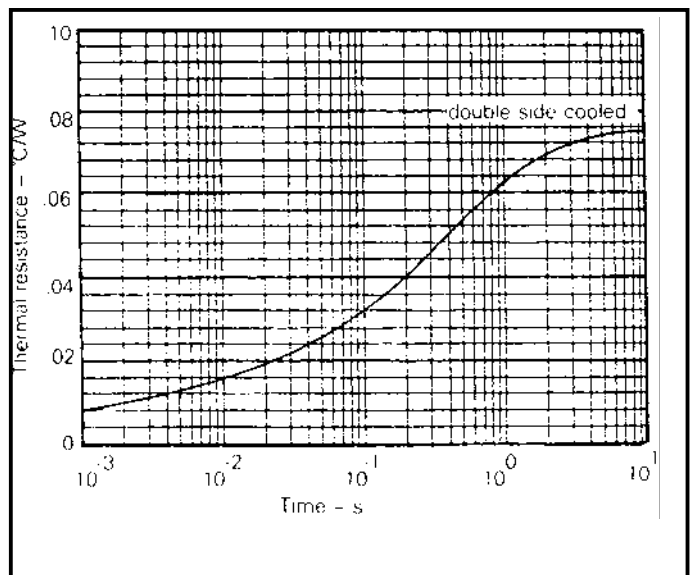


Fig.5 Maximum (limit) transient thermal resistance

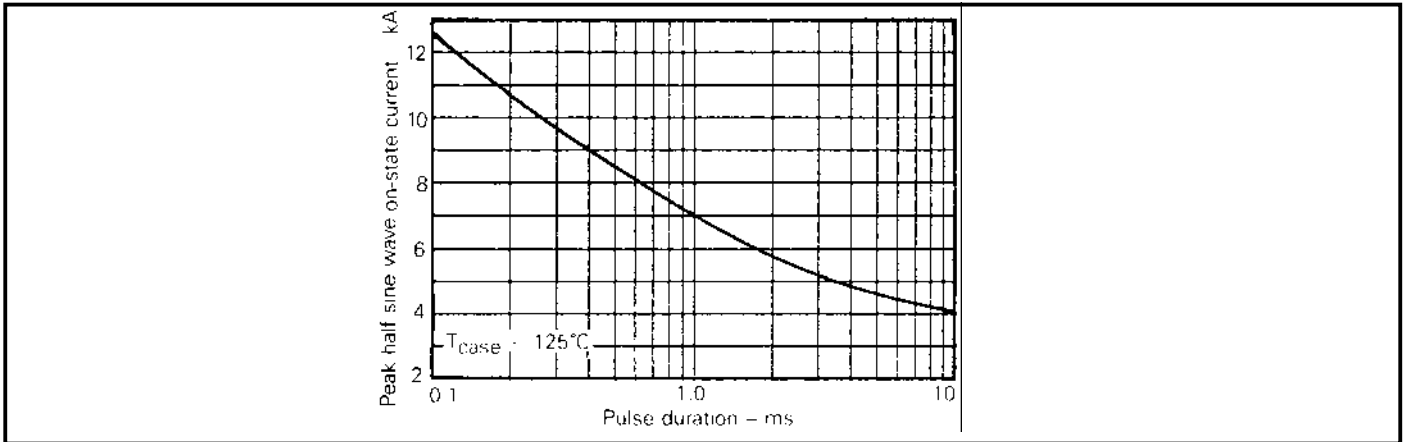


Fig.6 Surge (non-repetitive) on-state current vs time

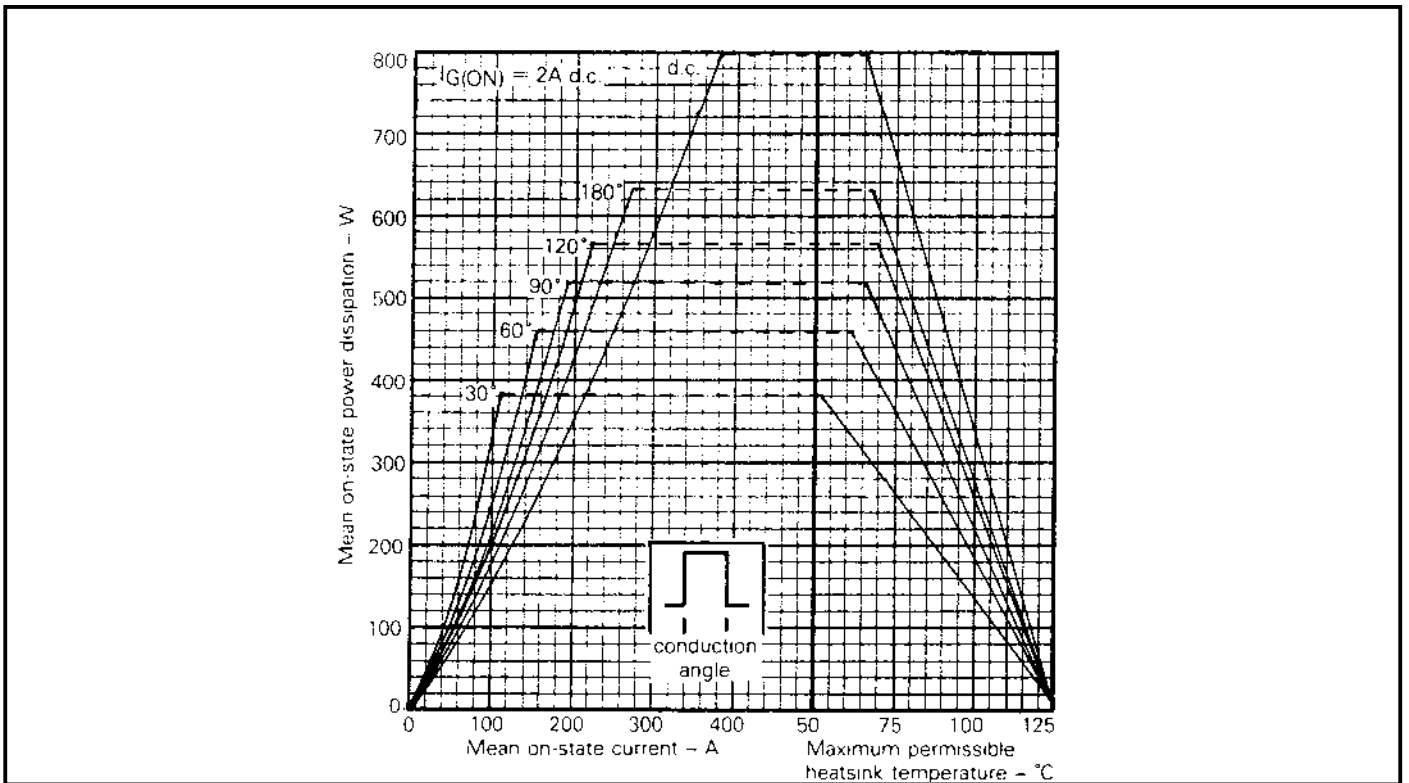


Fig.7 Steady state rectangular wave conduction loss - double side cooled

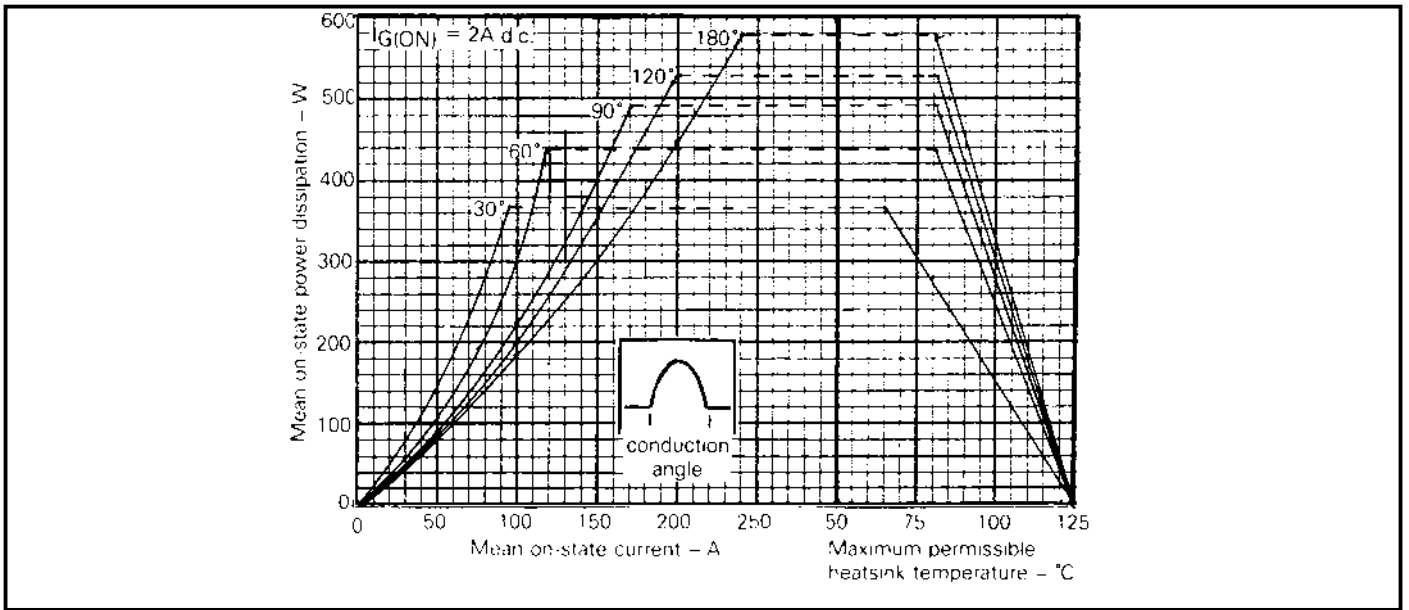


Fig.8 Steady state sinusoidal wave conduction loss - double side cooled

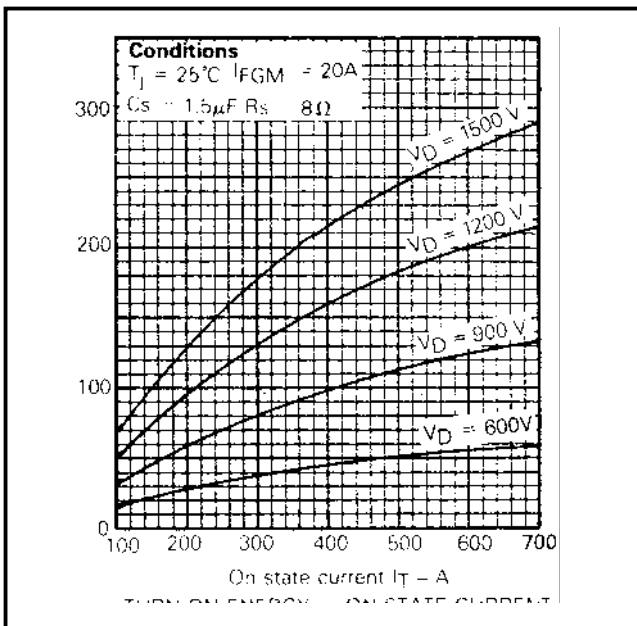


Fig.9 Turn-on energy vs on-state current

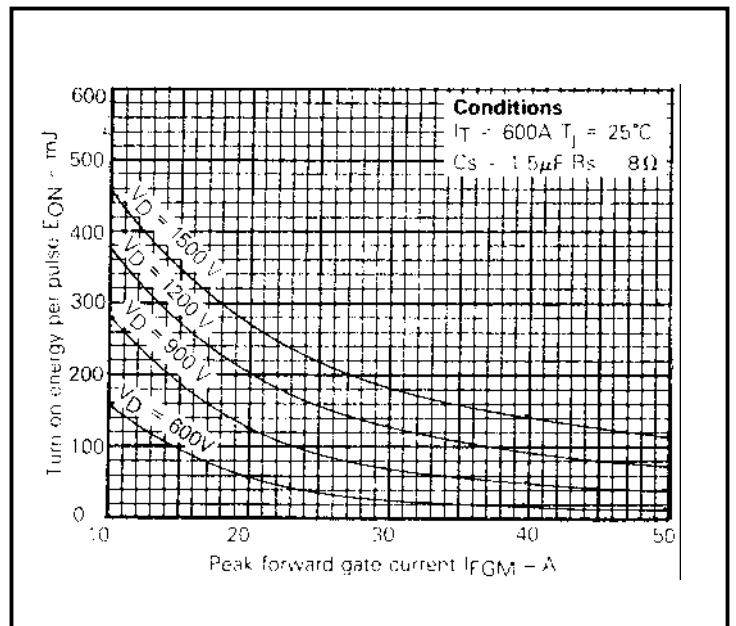


Fig.10 Turn-on energy vs peak forward gate current

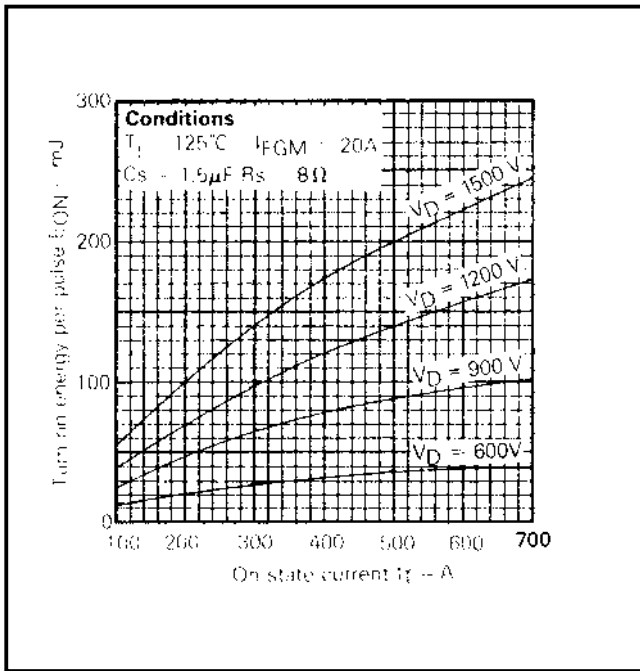


Fig.11 Turn-on energy vs on-state current

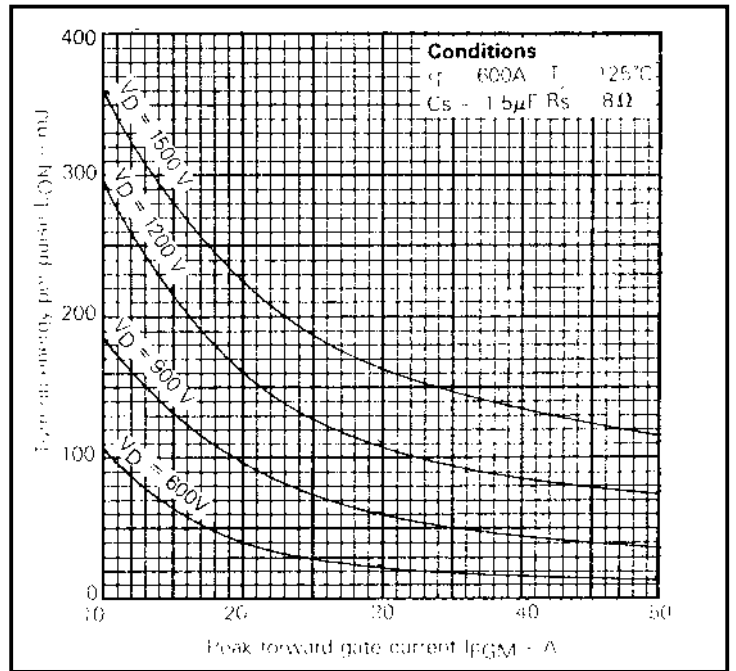


Fig.12 Turn-on energy vs peak forward gate current

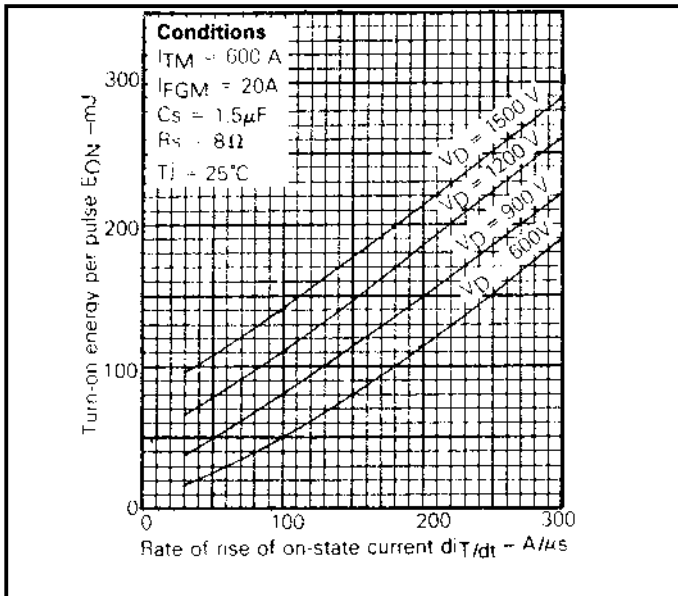


Fig.13 Turn-on energy vs rate of rise of on-state current

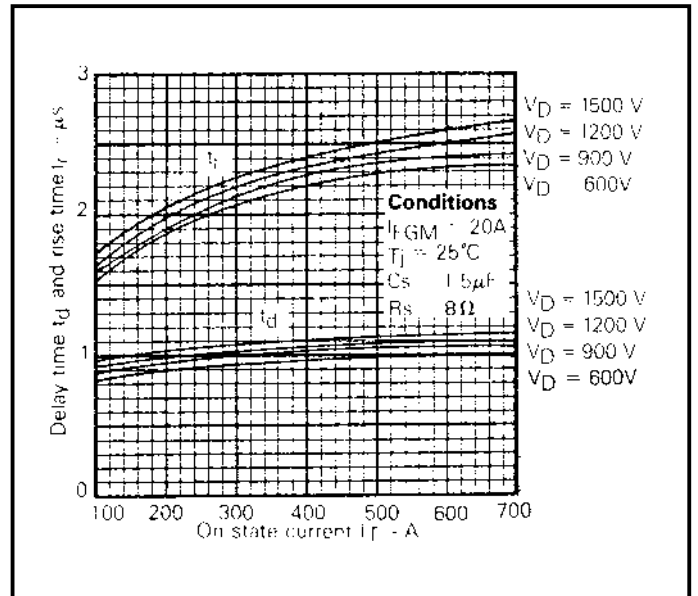


Fig.14 Delay time and rise time vs on-state current

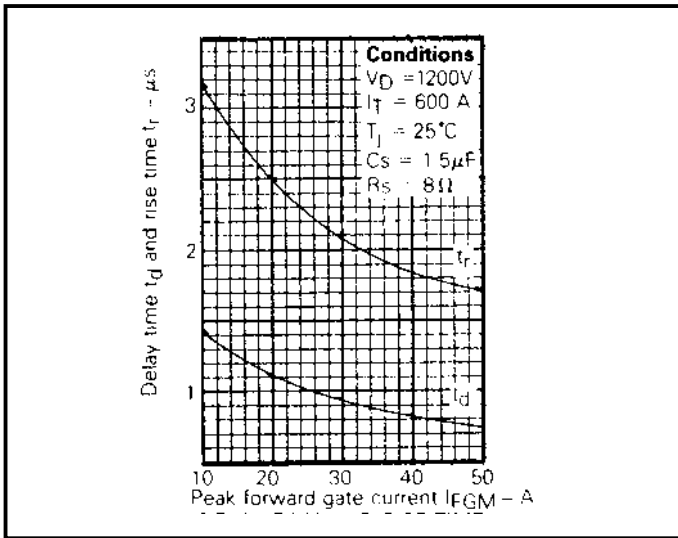


Fig.15 Delay time and rise time vs peak forward gate current

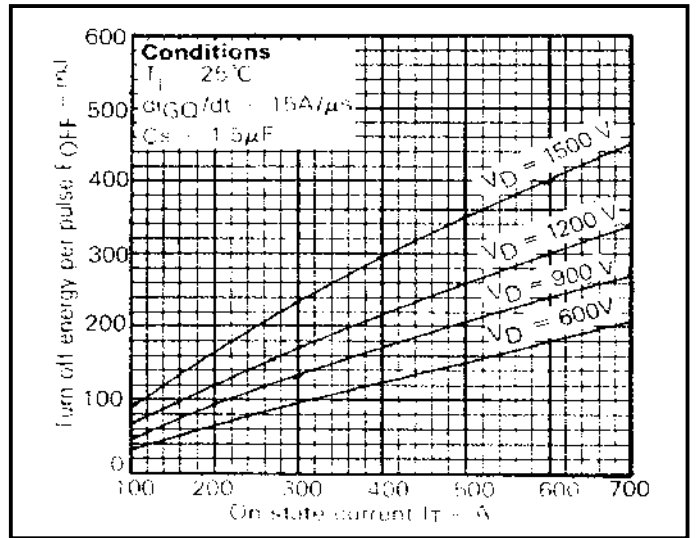


Fig.16 Turn-off energy vs on-state current

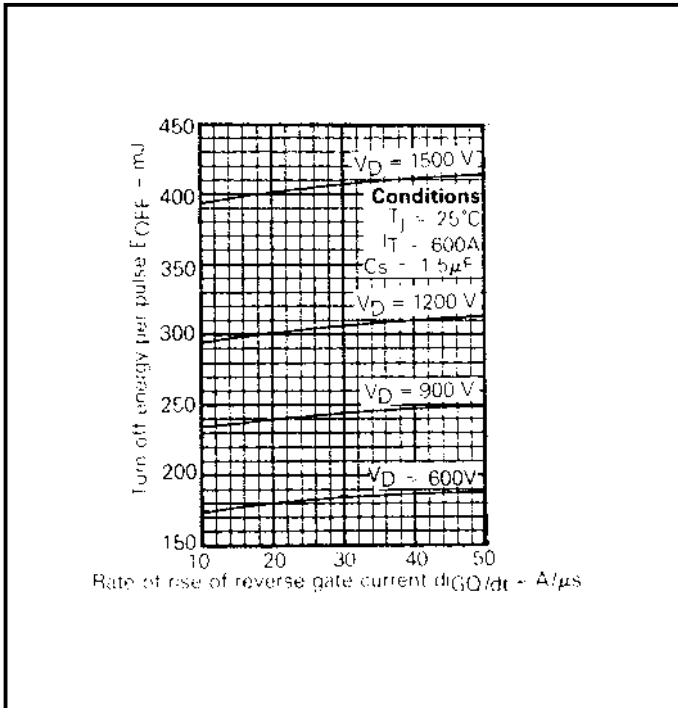


Fig.17 Turn-off energy vs rate of rise of reverse gate current

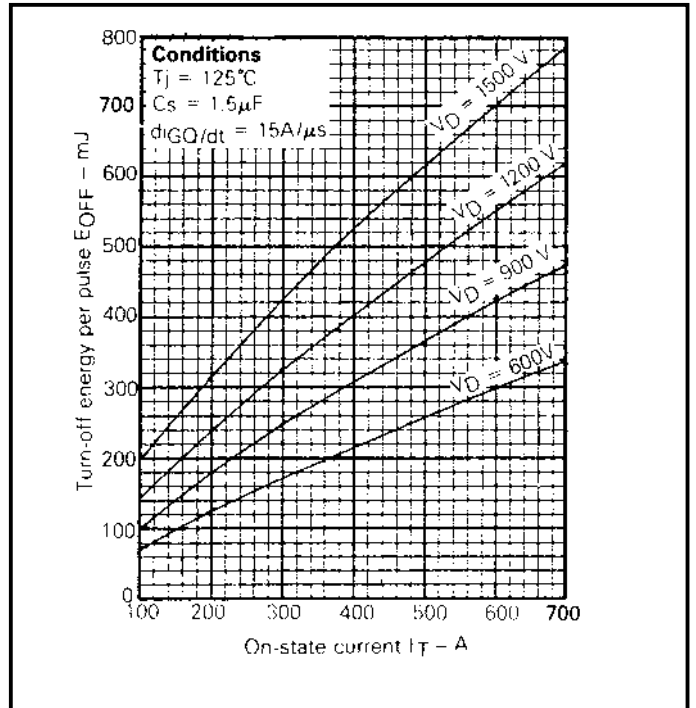


Fig.18 Turn-off energy vs on-state current

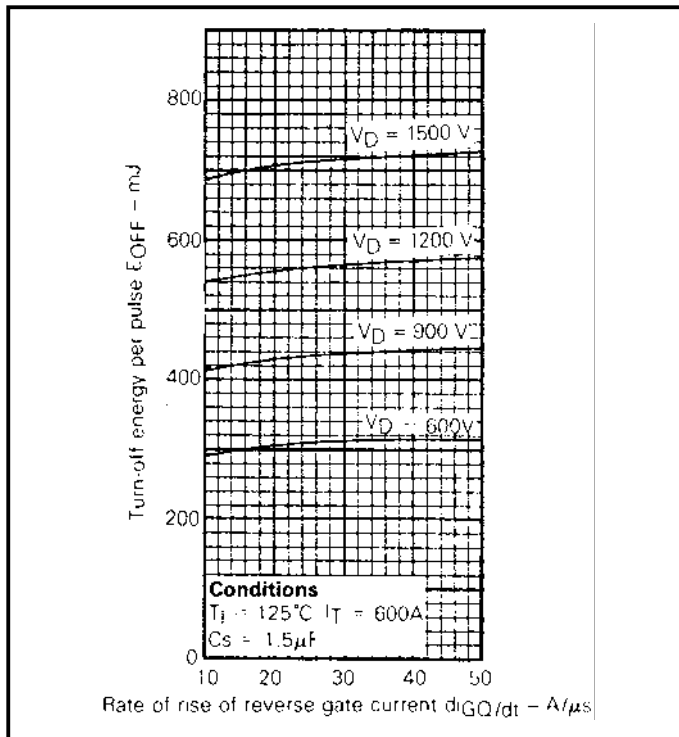


Fig.19 Turn-off energy vs rate of rise of reverse gate current

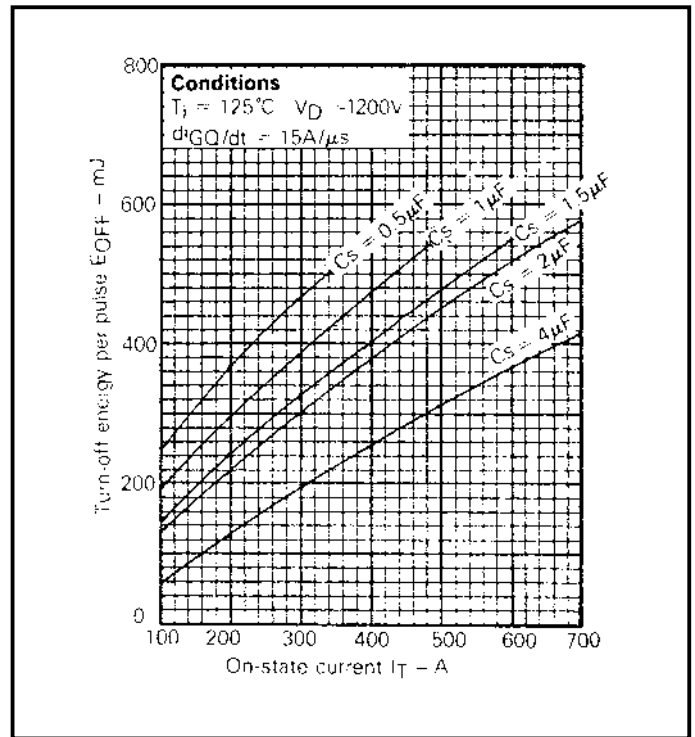


Fig.20 Turn-off energy vs on-state current with C_s as parameter

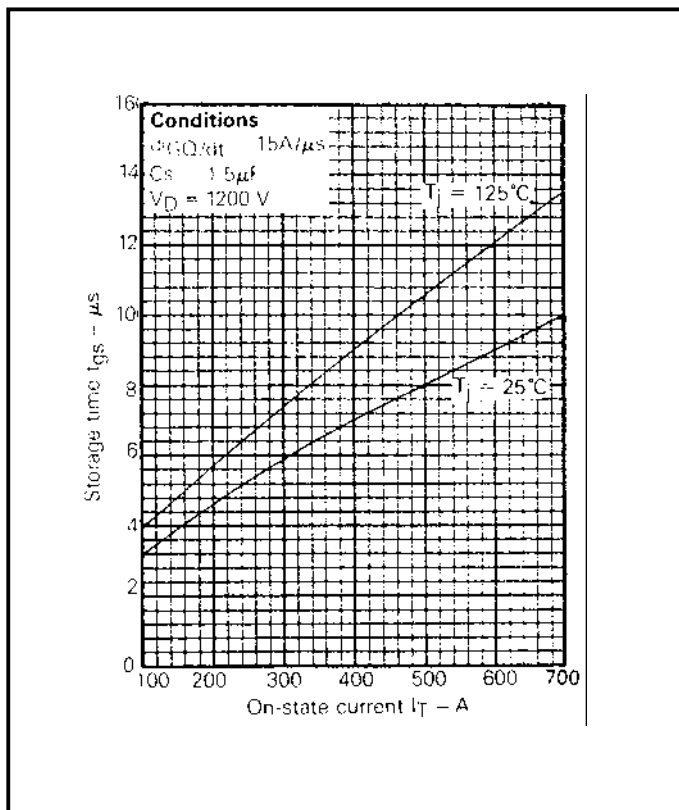


Fig.21 Storage time vs on-state current

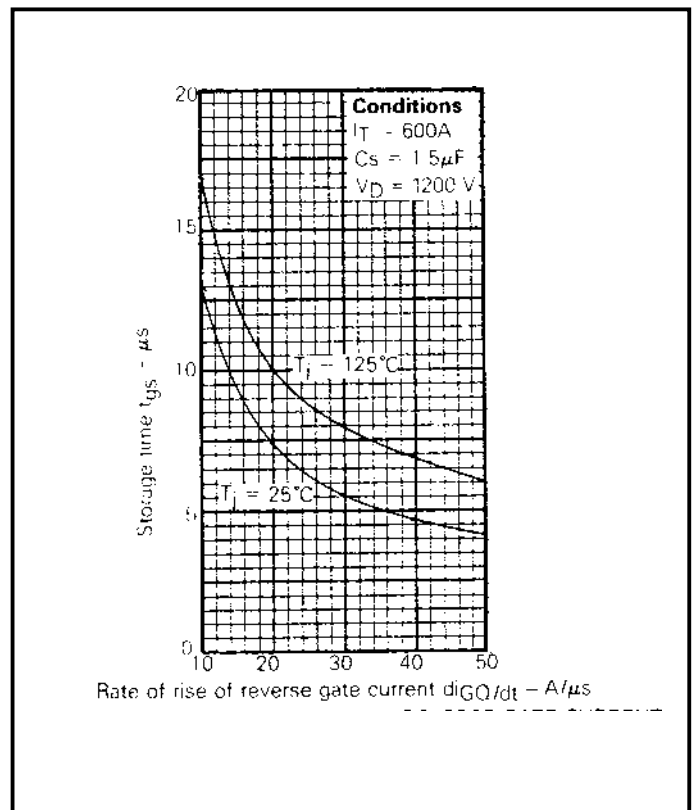


Fig.22 Storage time vs rate of rise of reverse gate current

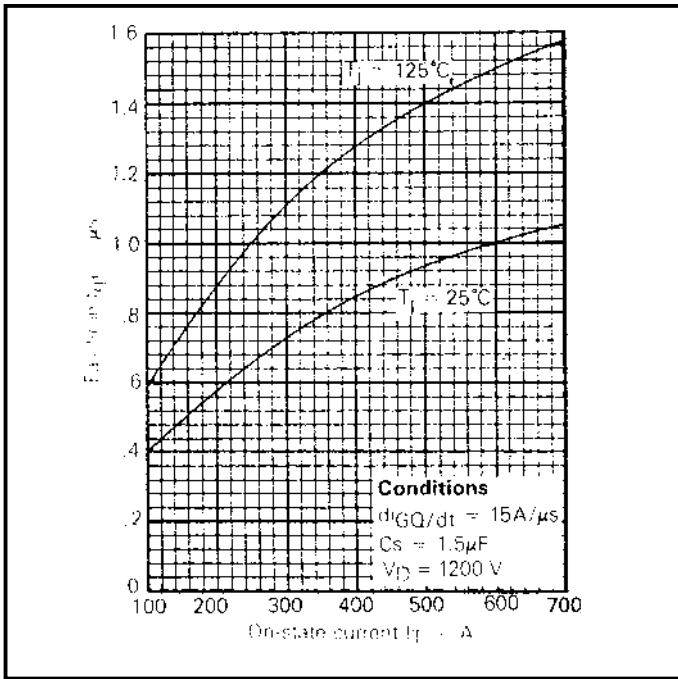


Fig.23 Fall time vs on-state current

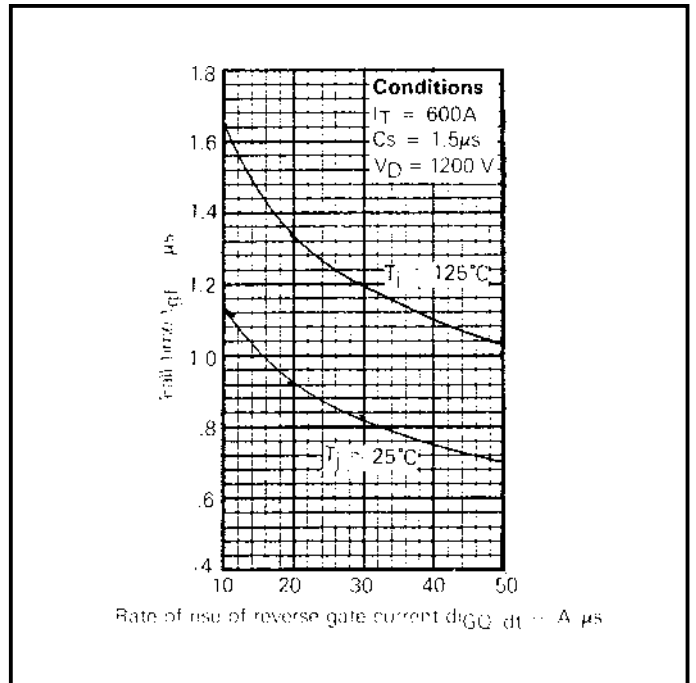


Fig.24 Fall time vs rate of rise of reverse gate current

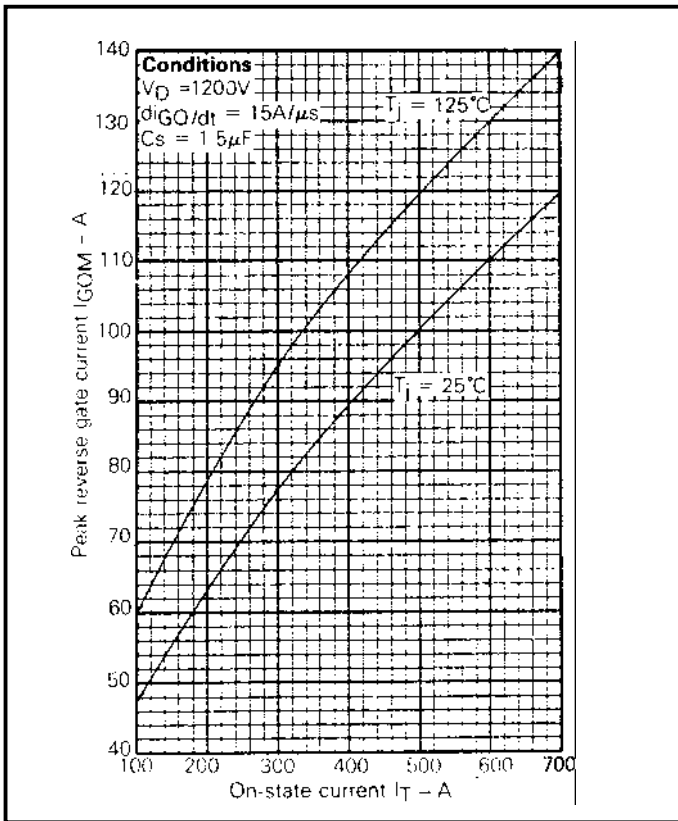


Fig.25 Peak reverse gate current vs on-state current

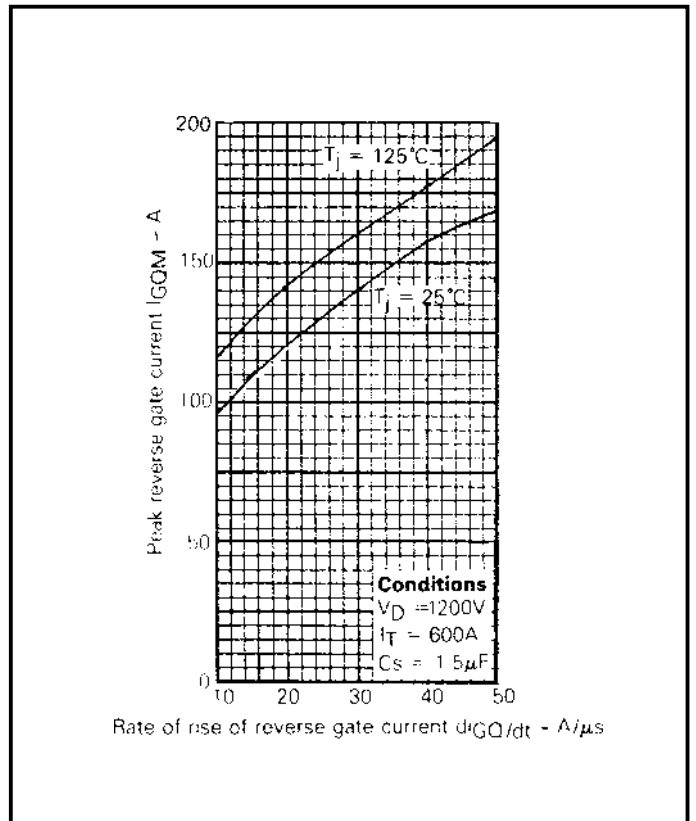


Fig.26 Peak reverse gate current vs rate of rise of reverse gate current

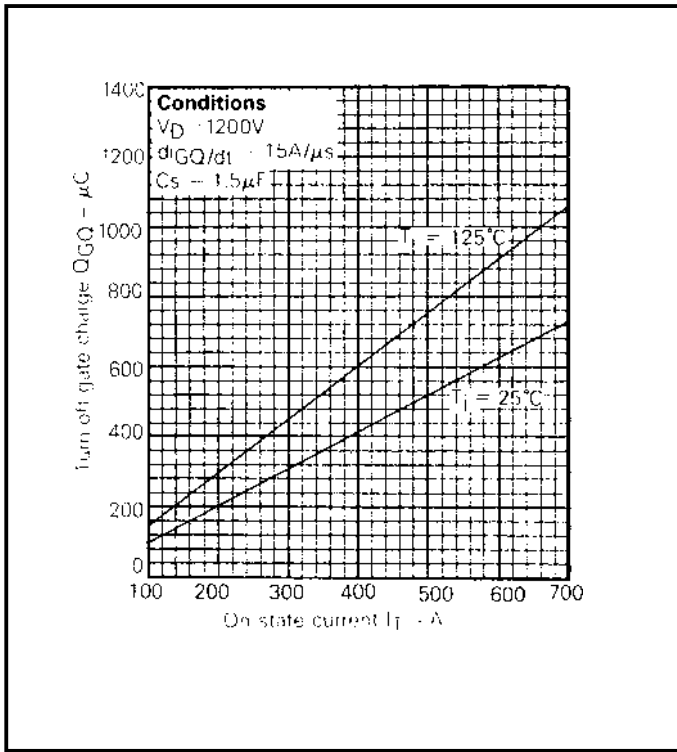


Fig.27 Turn-off gate charge vs on-state current

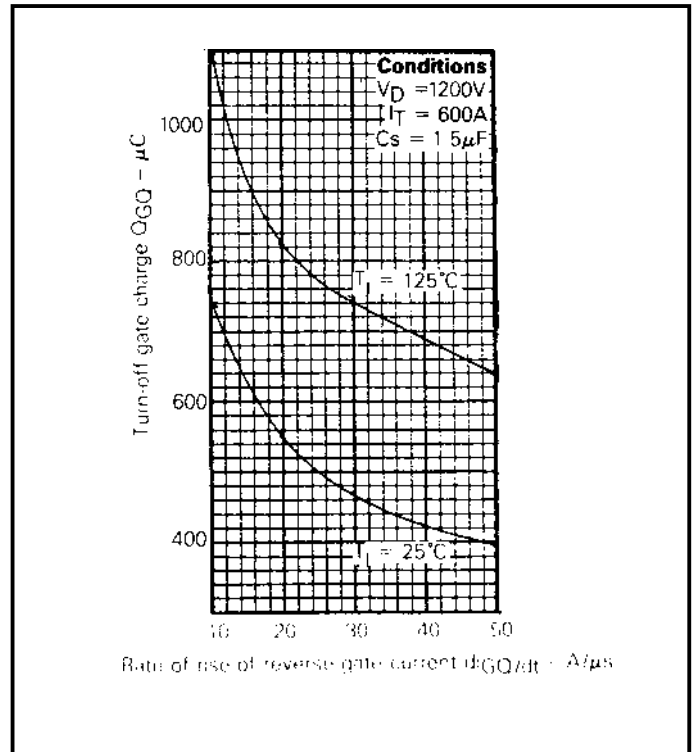


Fig.28 Turn-off gate charge vs rate of rise of reverse gate current

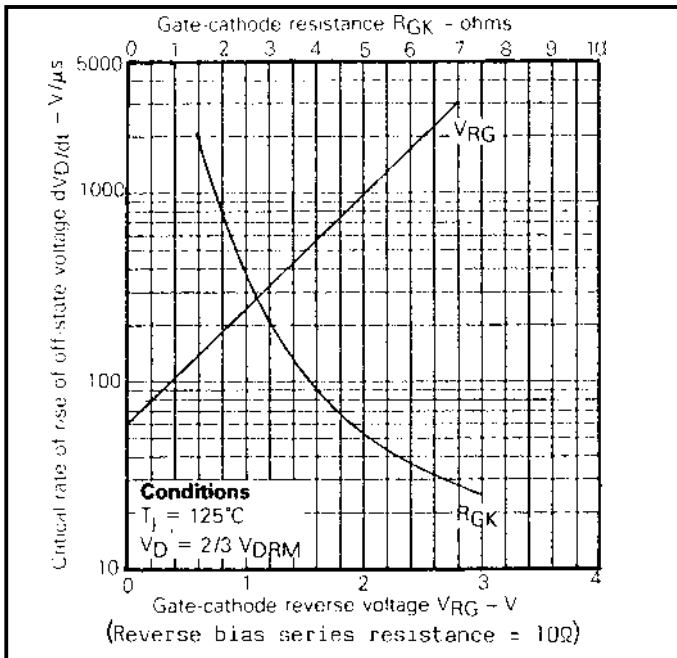
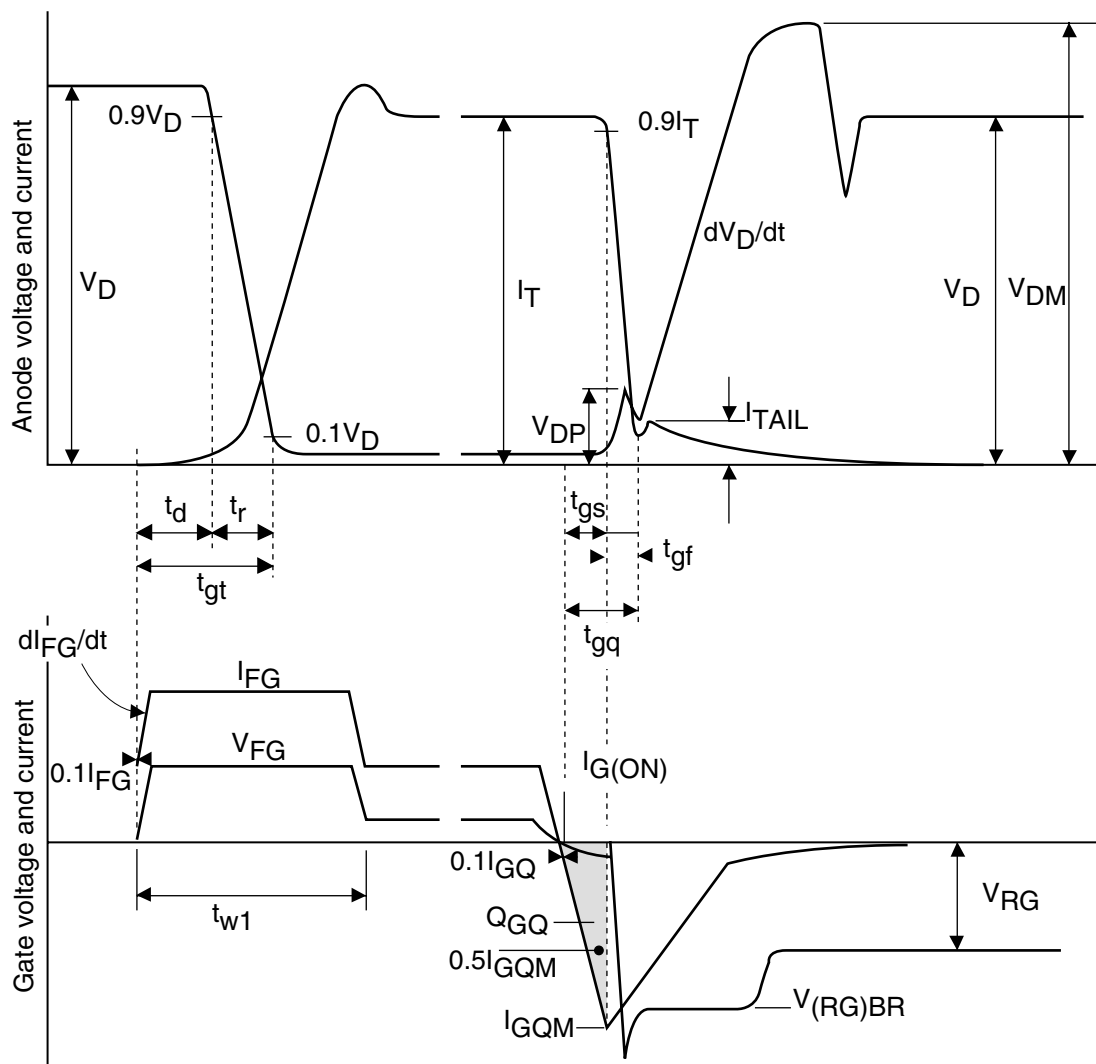


Fig.29 Dependence of critical dv_D/dt on gate-cathode resistance and gate-cathode reverse voltage

Snubber Capacitor C_s (μF)	Snubber Resistor R_s (Ω)	Minimum Reset Time (μs)
2	7	35
	5	30
15	7	26
	5	22
1	7	17
	5	15

Table of snubber discharge time variation with snubber capacitor value.



Recommended gate conditions:

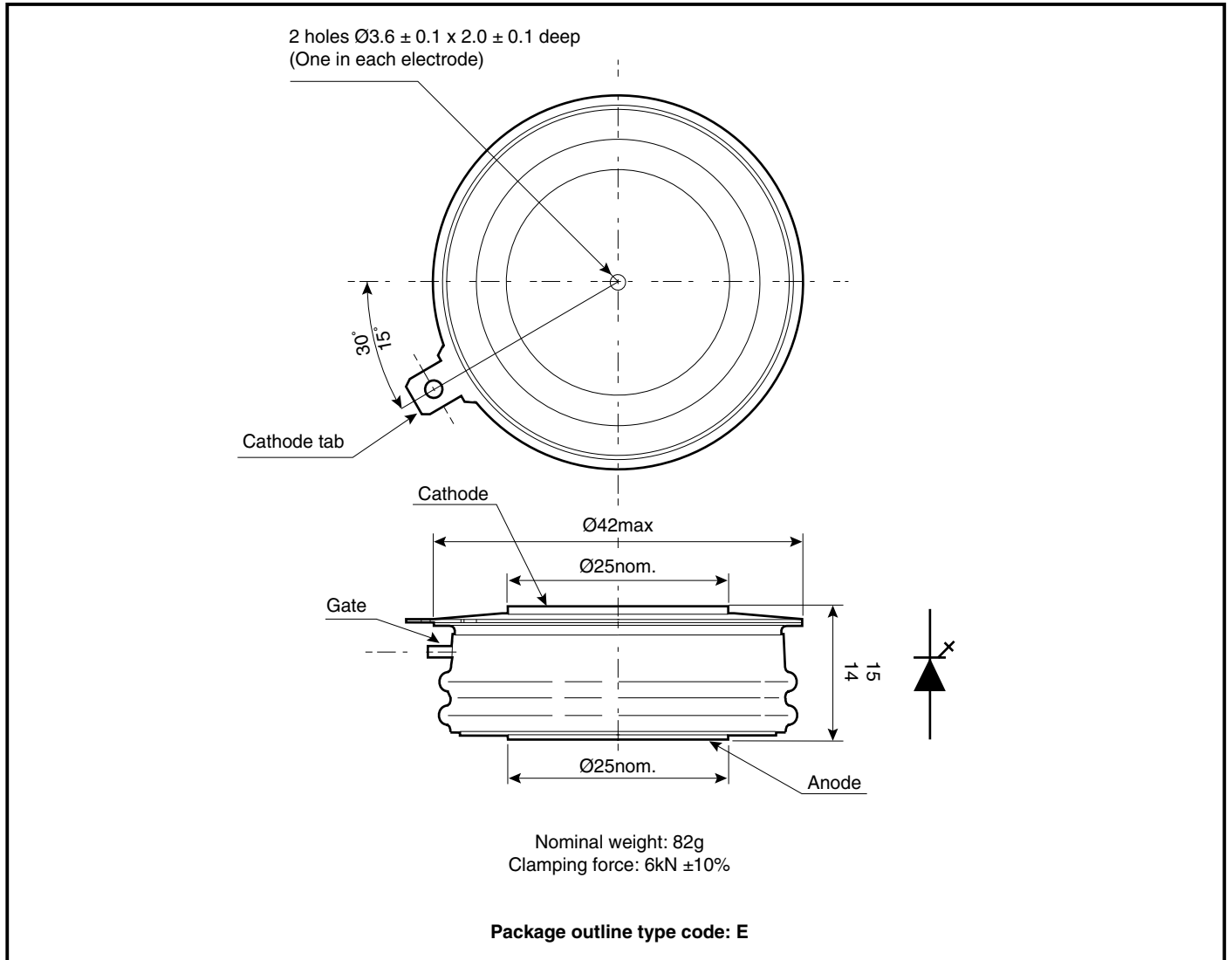
- $I_{TCM} = 600A$
- $I_{FG} = 20A$
- $I_{G(ON)} = 2A \text{ d.c.}$
- $t_{w1(\text{min})} = 4.5\mu s$
- $I_{GQM} = 130A$
- $di_{GQ}/dt = 15A/\mu s$
- $Q_{GQ} = 900\mu C$
- $V_{RG(\text{min})} = 2V$
- $V_{RG(\text{max})} = 16V$

These are recommended Dynex Semiconductor conditions. Other conditions are permitted according to users gate drive specifications.

Fig.30 General switching waveforms

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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